The SLICE Initiative: Towards a Shared Infrastructure for ML EDA

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Supported by:

Team Members

Academic partners:

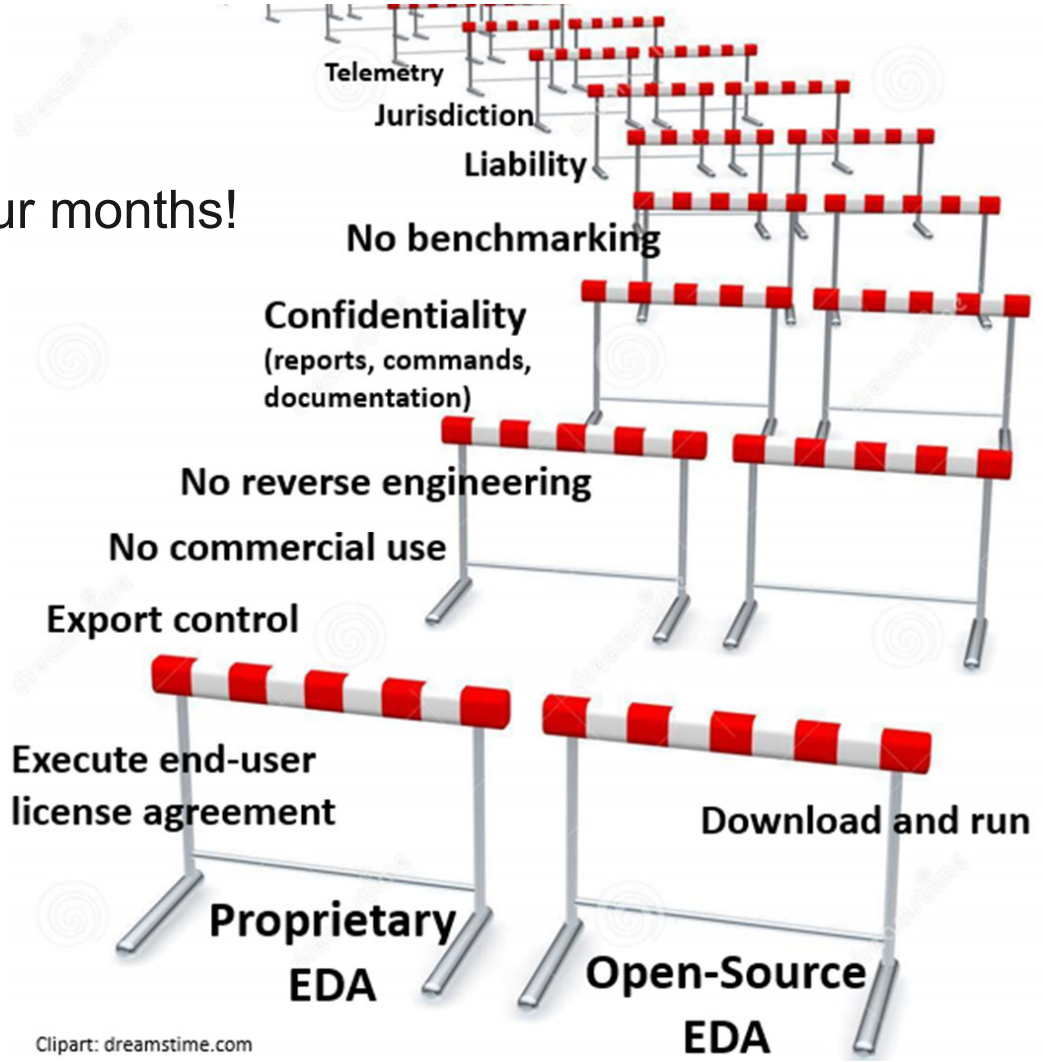
- Texas A&M University
- New York University
- University of Minnesota
- University of California, San Diego
- Duke University
- Georgia Tech
- Arizona State University
- etc.

Industry partners:

- Efabless
- CHIPS Alliance

Barriers to MLEDA adoption

- 2/3 development time on preparing training/test data
- 3 hours a design flow, 1000 data samples require four months!
- 74 days for obtaining data on 20 analog circuits
- Each team starts from scratch, repeated efforts
- Results from different teams not comparable
- Low reproducibility by other teams
- Lack of a shared open infrastructure including EDA tools, PDKs, libraries and datasets



A. B. Kahng “A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping” ICCAD 2022

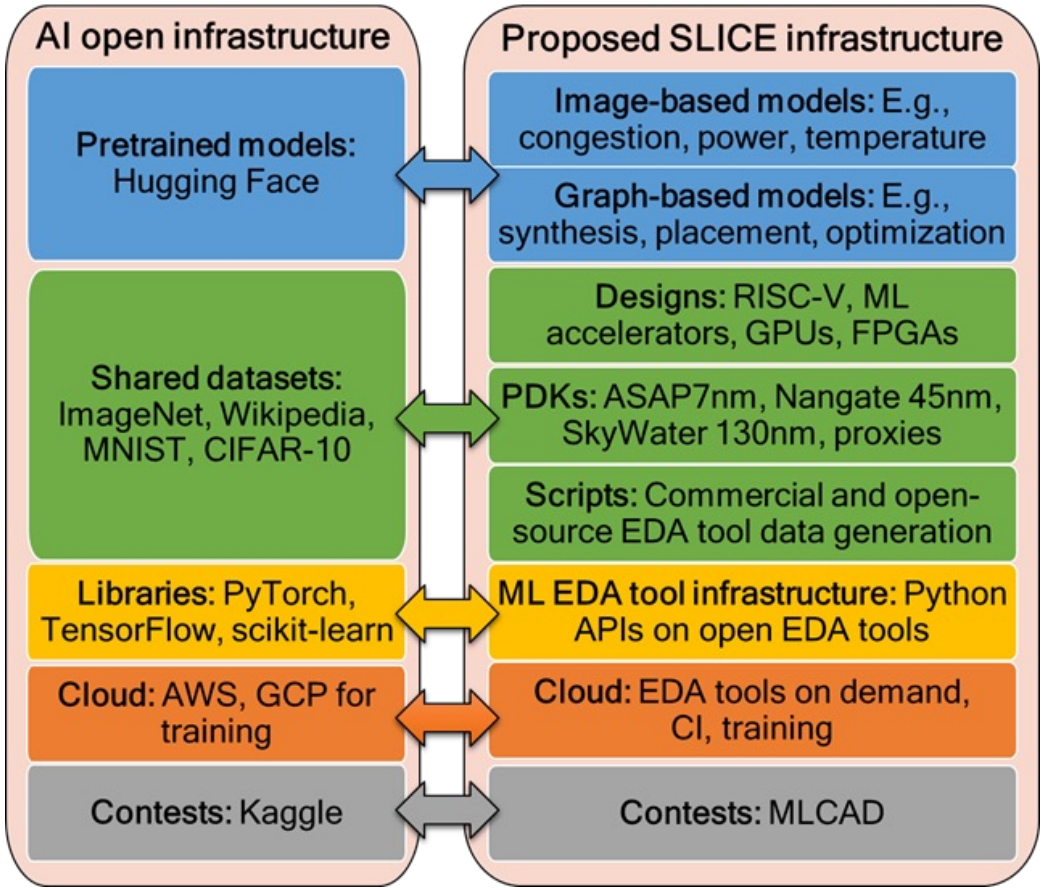
NSF Workshop on Shared Infrastructure for ML EDA

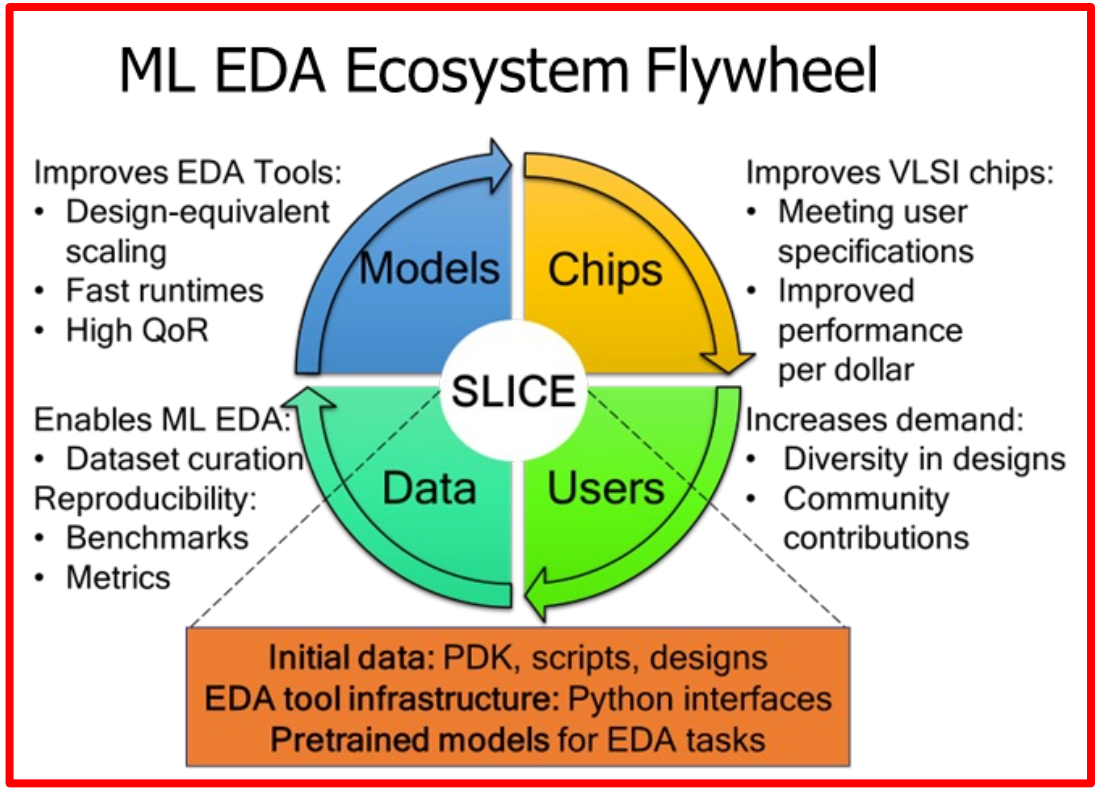
Minneapolis, March 10, 2023

> 70 attendees from 25 universities and 11 companies

SLICE: A Shared Machine Learning Infrastructure for the Community of EDA

Learning from the ML Community





The SLICE Initiative: Website

SLICE Contents

SLICE serves as a one-stop shop and has sourced together several existing efforts for benchmarking, dataset collection, tutorials, and has incorporated into its GitHub repostories as a part of SLICE-ML-EDA organization.

- SLICE MLCAD 2023 Presentation
- Datasets
- EDA Tool Flows
- Contests
- Open-source PDKs
- NSF Workshop on Shared Infrastructure for ML EDA
- NSF Workshop Report

https://slice-ml-eda.github.io/

ML EDA Contests

SLICE has curated a list of contests that have encouraged the use of machine learning techniques in EDA

- MLCAD 2023 FPGA Macro Placement
  - Towards academic research for developing ML or deep RL approaches to improve upon the current state-of-the-art macro placement tools.
- ICCAD 2023 Problem C ML for IR Drop
  - Advacning ML-based IR drop prediction and providing a standard set of benchmarks for training and evaluation.
- ISPD 2024 GPU/ML-enhanced Large Scale Global Routing
  - Goal is to stimulate academic research aimed at developing a GPU/ML-enhanced global router tailored for industrial-level circuits
- ICCAD 2024 Logic Gate Sizing Using ML
  - Goal is to incentivize the use of ML and GPU-acceleration for logic gate sizing.

Conclusions

- Shared infrastructure is critical for
  - Fast ML EDA progress
  - Spin of ecosystem flywheel
- Resource investment
- Academia-industry collaboration
- Community driven-effort is essential