Karlsruhe Institute of Technology

Open-source EDA efforts in Germany: AI HW-SW Co-design and Other Projects

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Federal Ministry
of Education
and Research

Funding program „Design Instruments for Sovereign Chip Develpoment with Open Source (DE:Sign)“

bmbf.de

Federal Ministry
of Education
and Research

DE:Sign |Overview

- Design tools, methods and chip designs
  focussed on open source
- Significant development of the tool chain
- Participation of young academics and talents
- Close collaboration with network „Chipdesign Germany“
- Industry- or science-driven, pre-competitive
  joint or individual R&D projects
- Universities, research institutions, companies

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DE:Sign |Research focus

a. Open source **EDA tools**, PDKs und IP libraries

b. Open source **design methods**

c. Novel **chip designs** based on open source EDA tools, PDKs andIP

d. Design tools, PDKs and IP for **novel technologies**

(e.g. chiplets, advanced packaging, MEMS, radio frequency)

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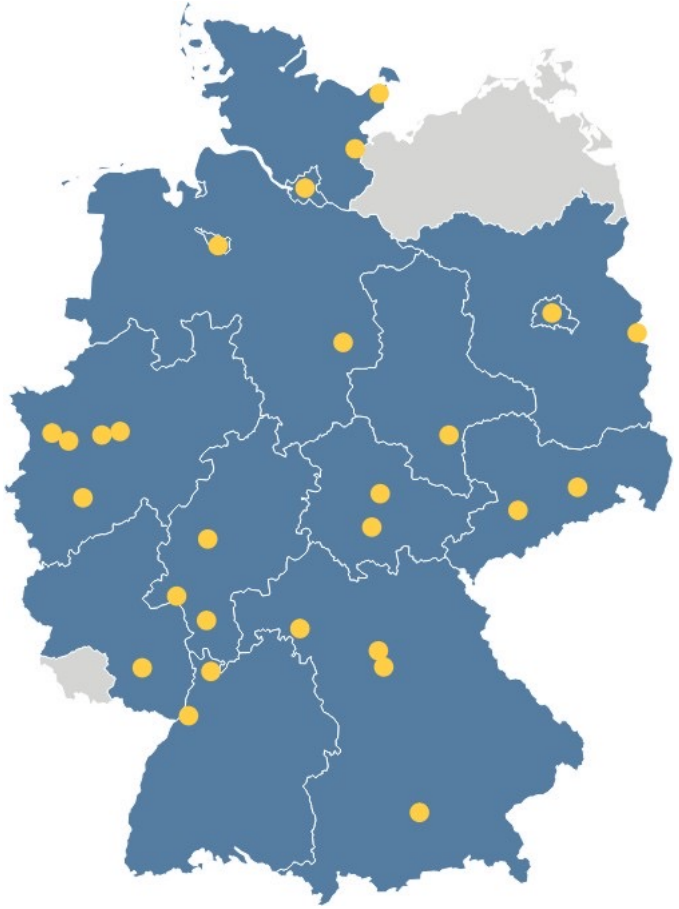
DE:Sign |Key figures

- **Deadline**: 31 July 2023
- **Submissions:** 36 pre-proposals
  with 150 partners (in total)
- **Selection meeting:** 29 September 2023
- **Selection:** 15 R&D projects with 62 partners (in total)
  (thereof 12 industrial partners)
- 11 joint projects, 4 individual projects
- **Grant (total):** 29.6 Mio. EUR



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DE:Sign |R&D projects open source EDA tools

Talents: Student competition „Open source chip design challenge“ (**OCDCpro**)

Analog design

- ✓ Text based design (**ORDeC**)
- ✓ High frequency chips (**DEMICO**)

Digital design

- ✓ eFPGAs (**OWAS**)
- ✓ FPGAs (**FEntWumS**)
- ✓ RISC-V (**GATE-V**)
- ✓ Verification (**OSVISE**)
- ✓ DRAM (**DERAMSys**)
- ✓ AI hardware (**EDAI**)

Hardware security

- ✓ HW architecture (**ExViPaS**)
- ✓ HW security module (**SIGN-HEP**)

Novel technologies

- ✓ RFETs (**ReDesign**)
- ✓ MEMS/ASIC (**Meta-X**)
- ✓ Packages/SiP (**PASSIONATE**)
- ✓ Radiation resistant HW (**Flowspace**)

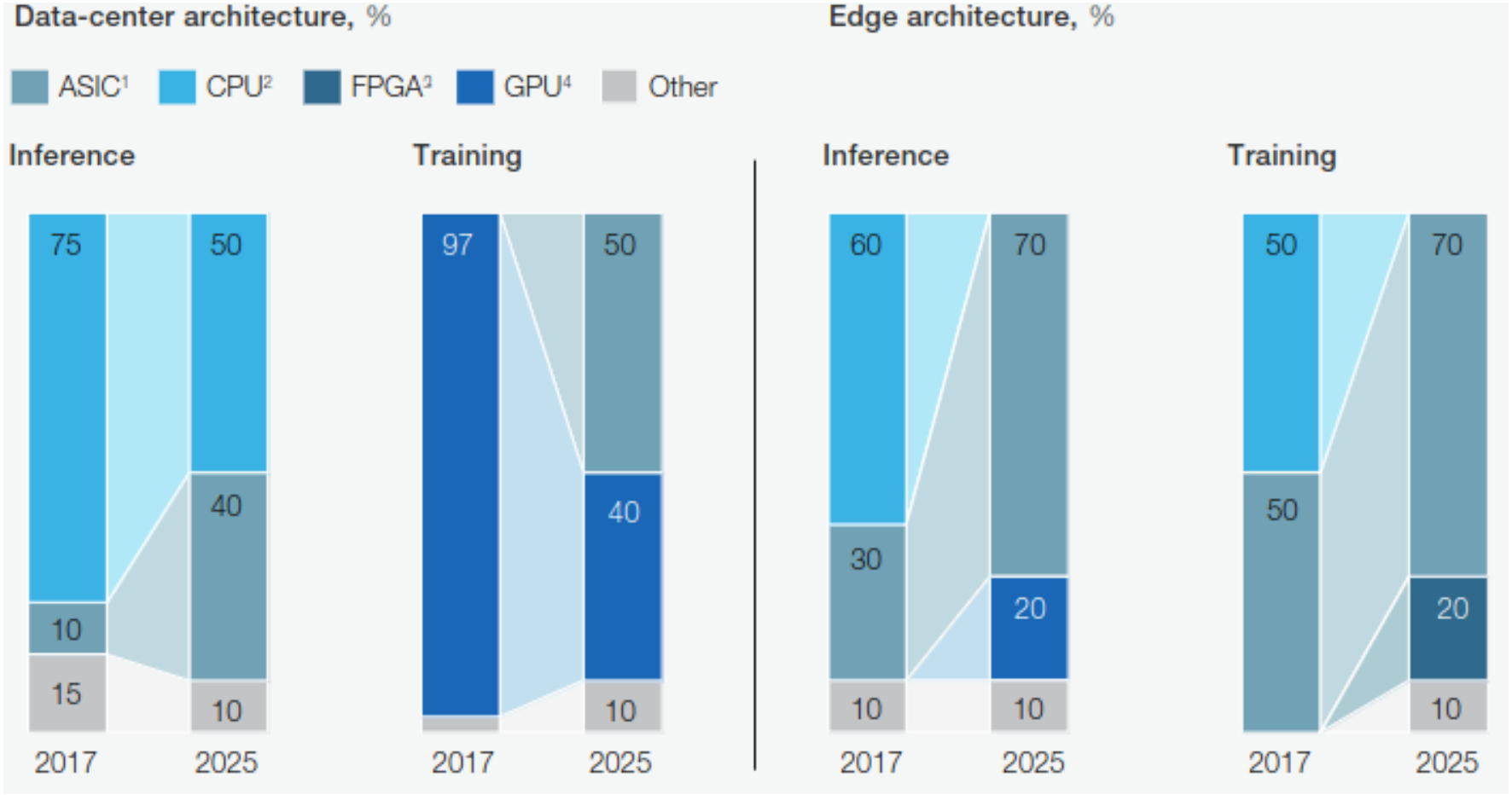
Open-source Design Tools for Co-development of AI Algorithms and AI Chips DI-EDAI

Bundesministerium
für Bildung
und Forschung

Challenges in Attracting Talent for Chip Design

- **Long Path to Success**
  - **Mastery Demands**
    - Requires deep understanding in various subjects
    - Deterring rapid-gratification seekers:
      - Missing “Hello World” moment for hardware design
- **Productivity vs Efficiency**
  - **Software vs Hardware**
    - Software productivity advancements: Assembly → C/C++ → Python
    - Hardware's focus on efficiency: hardware programming (languages) are cumbersome
- **Salary Gap**
  - **Compensation Disparity**
    - Lower salaries compared to software/AI
    - Dissuades potential talent

Shift of preferred HW in data centers and the edge

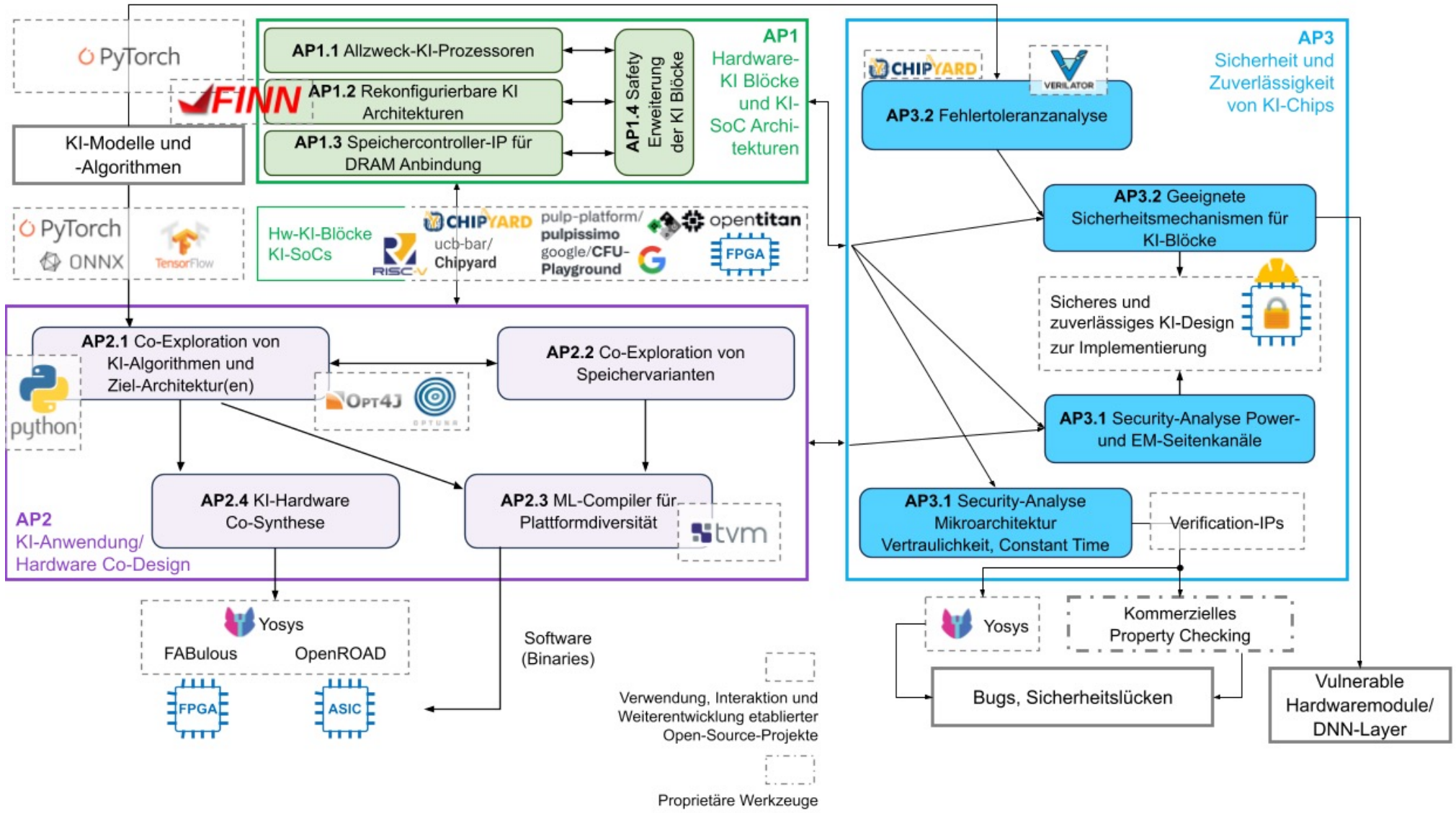


Source: McKinsey analysis 2018, Artificial-intelligence hardware: New opportunities for semiconductor companies

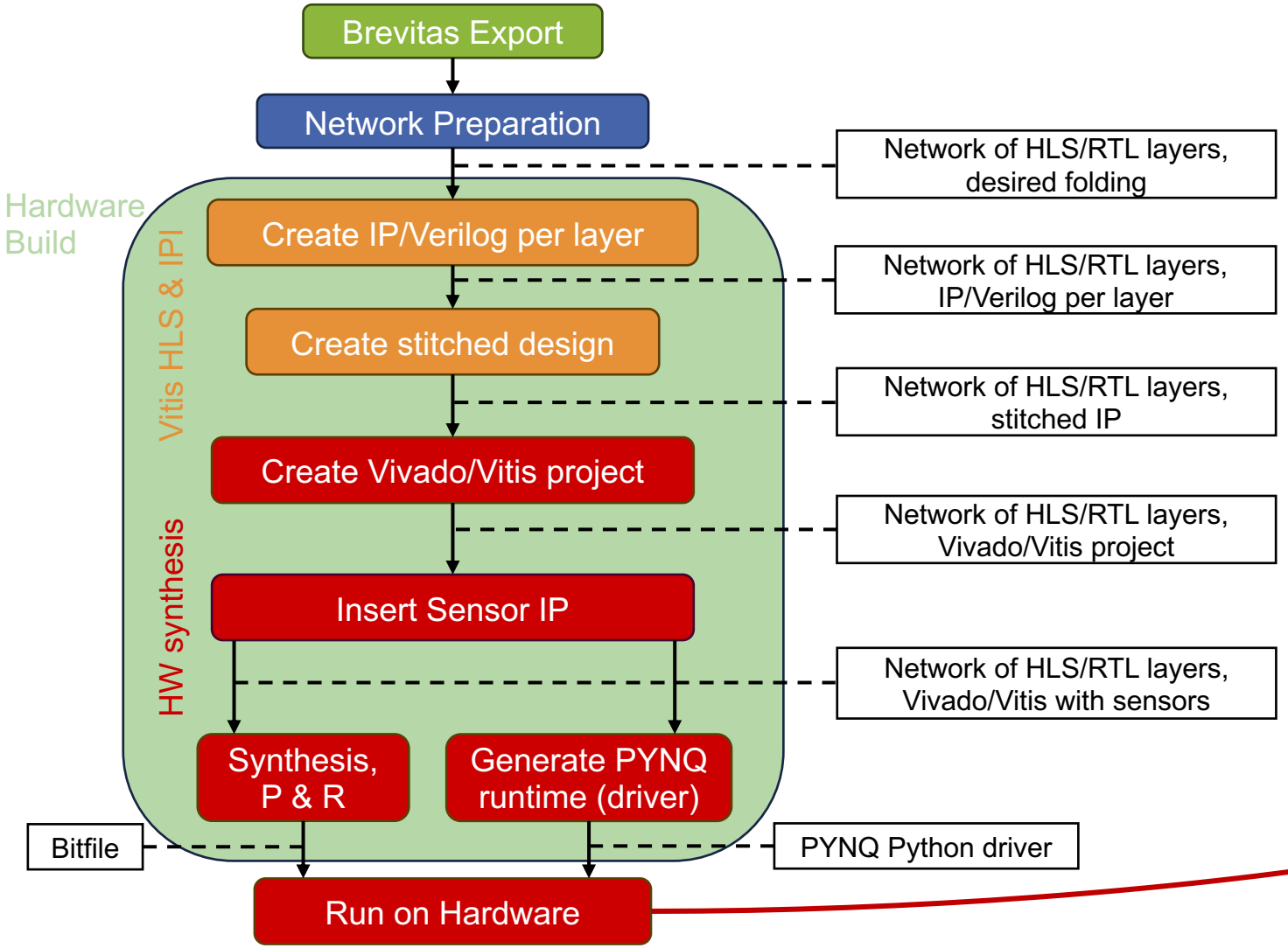
Challenges (and Solutions)

- **Goal:** Closing the gap between software and hardware side of AI
  - Productivity: like software development
  - Efficiency: coming from co-design)
- **Sustainability of open-source tools and ecosystems**
  - How to ensure open source ecosystem survives and thrives beyond initial funding?
  - **Community building** → education and training
  - **Large user base**: heavily used in teaching modules and lab
  - **Business model** around open source hardware EDA and design
- **Industry adoption**
  - **Complementing** rather than competing with existing EDA tools (and industry)
  - **Benchmarking** → quantifying added-value
  - Path: Academia → SME → (new) large design companies
- **Access to restricted technology**
  - Technology-agnostic design
  - Built on top of existing EDA and PDK

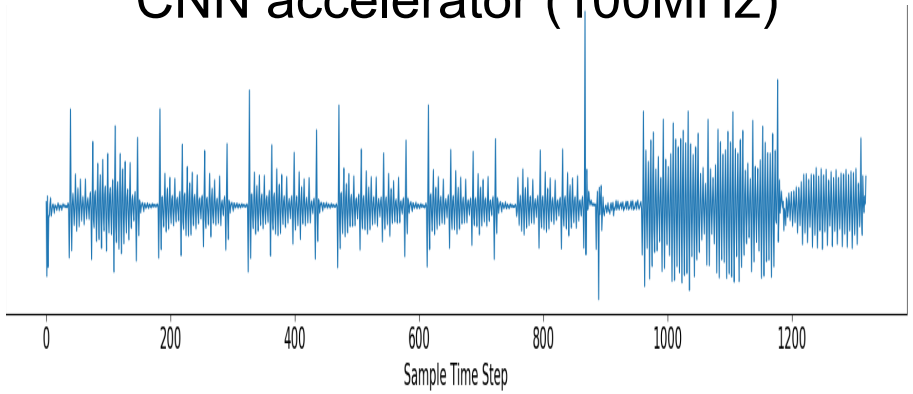
EDAI Approach



Voltage Fluctuation Sensor Integration in FINN

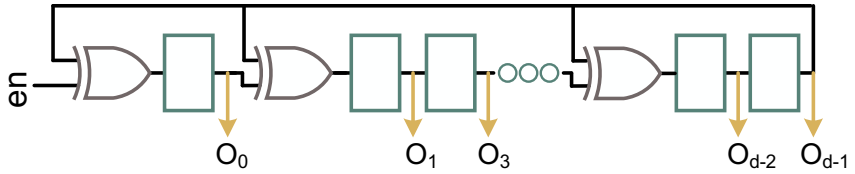


Measurement (200MHz) of a FINN-CNN accelerator (100MHz)

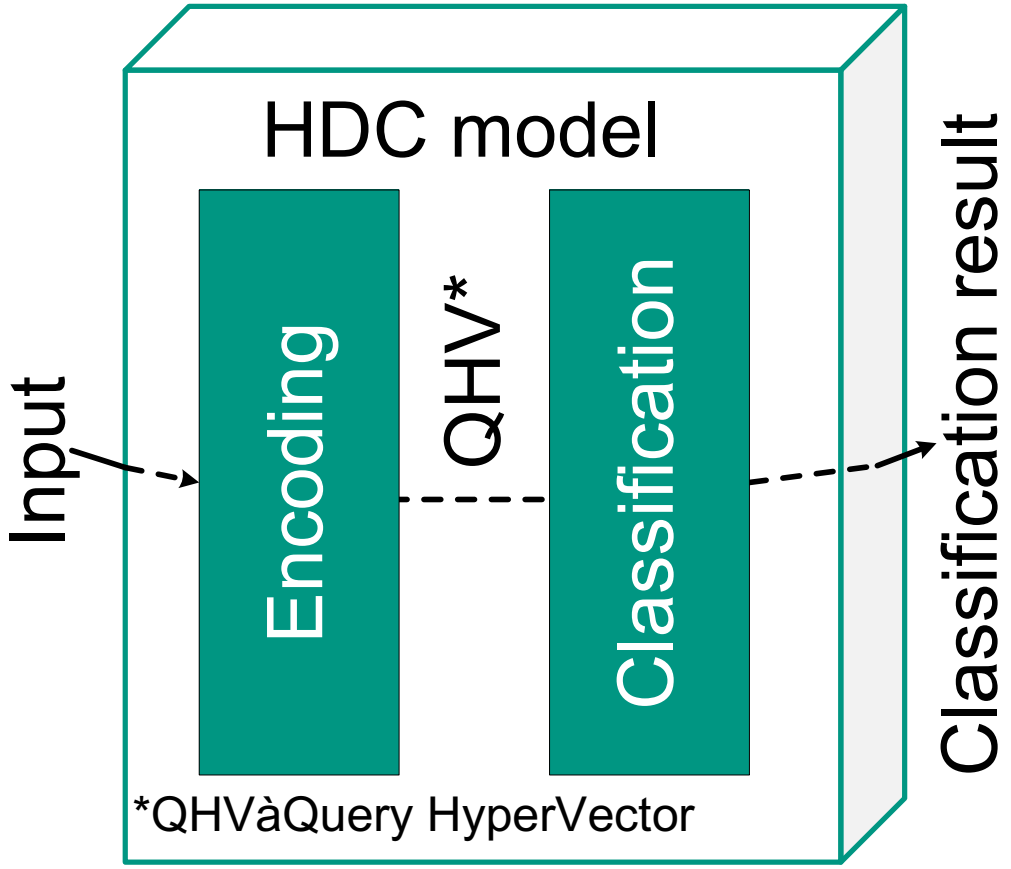


Open-Source Hyperdimensional Computing on FPGA

- A machine learning method
  - Can be used on Edge devices i.e, IoTs
- Data and calculations are represented
  - In a hyperdimensional space
- Benefits
  - Robustness
  - Can be trained on small datasets
  - Hardware-friendly operations:
- Our extensions
  - End-to-end framework, similar to FINN
  - Generating encoding parameters On-the-fly at runtime
  - Utilizing a combination of well-known cyclic array



  - Without sacrificing the accuracy



Industry Partners

SMEs

Large Industries (Design and EDA)

End Users