CircuitNet Dataset for ML in EDA: Where are We and Where to Go

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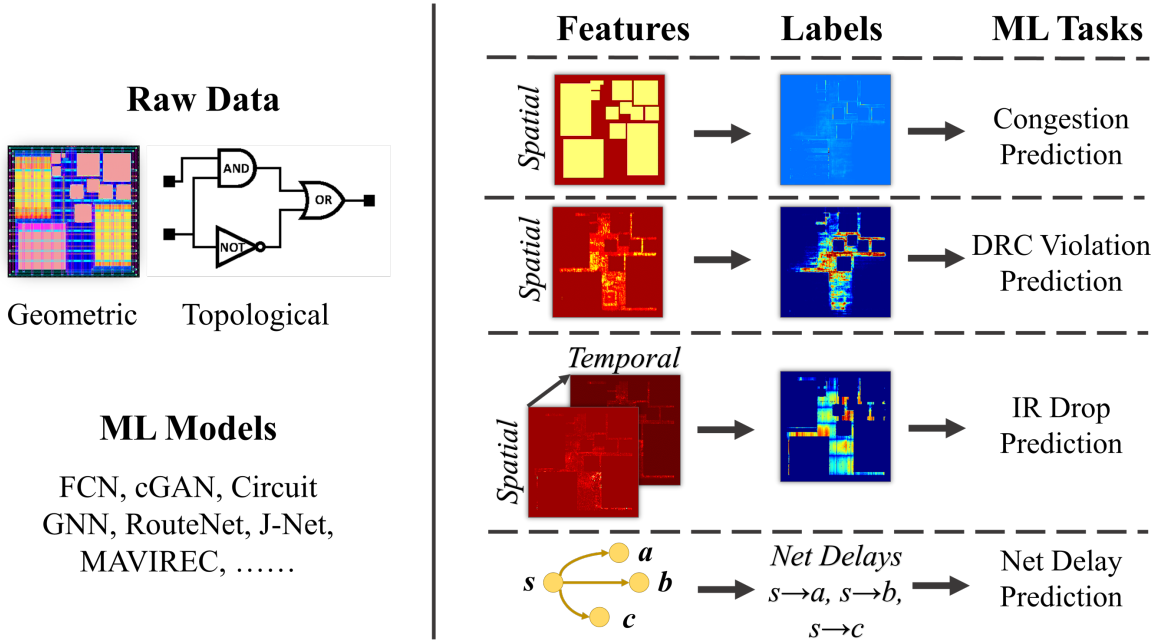
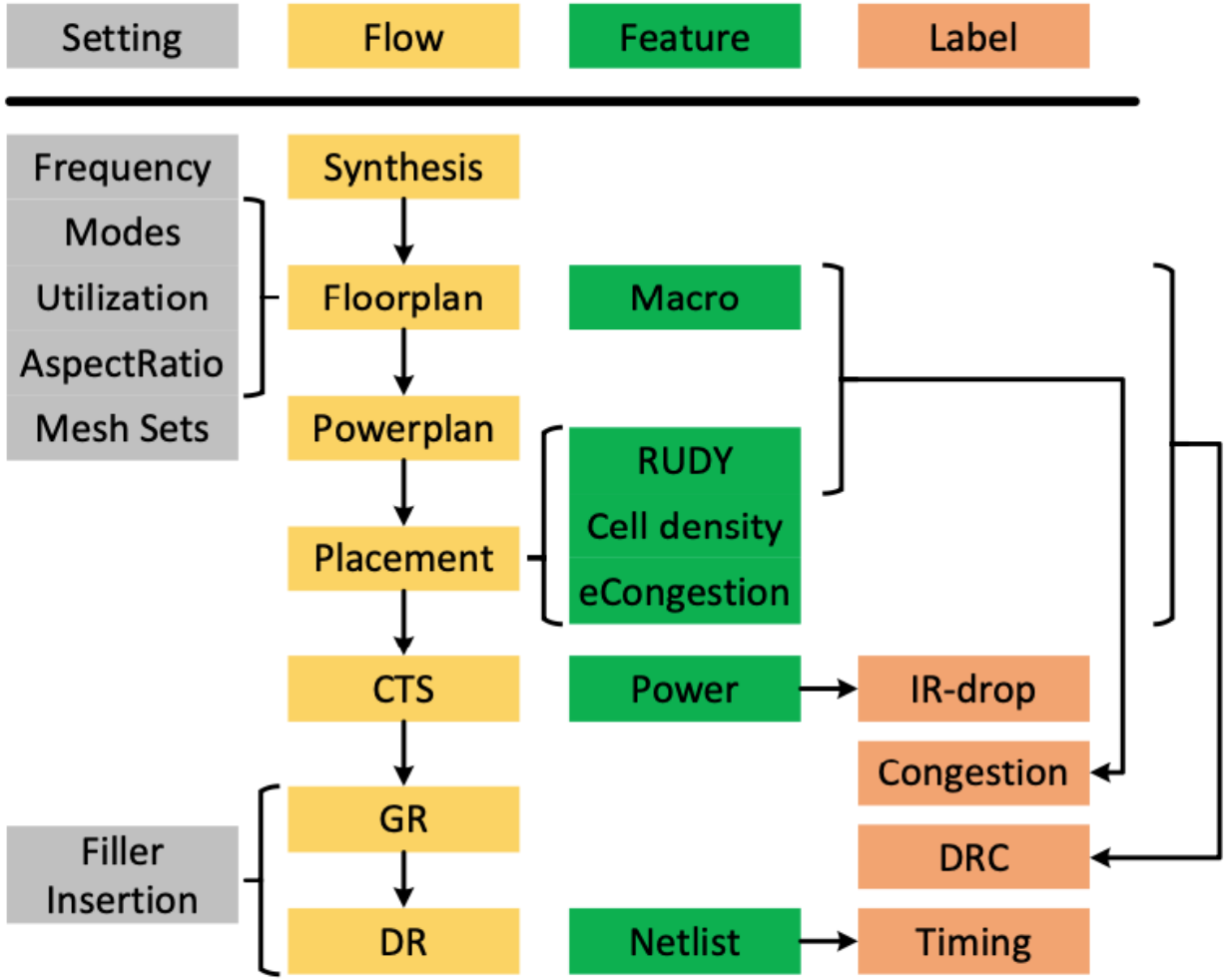
CircuitNet: ML for EDA Dataset [SCIS'22, TCAD'23, ICLR'24]

- 20K+ samples
  - CPU, GPU, AI accelerator designs
  - (PULPino, OpenC910, Vortex, NVDLA, ...)
  - Million-cell netlists
  - Real flow & PDK, e.g., 28nm, 14nm
- Support multiple tasks
  - Routability
  - IR drop
  - Timing
- Dataset & tutorial
  - https://circuitnet.github.io/
  - https://github.com/circuitnet/CircuitNet



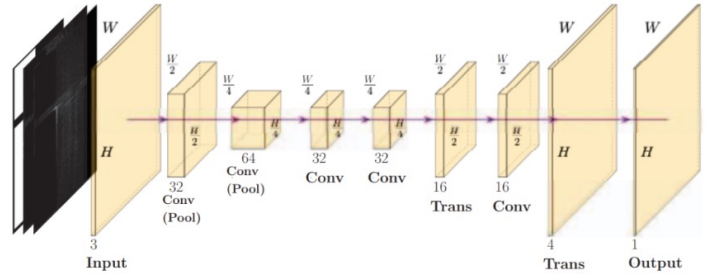
What's in CircuitNet



Numpy arrays, Verilog&LEF&DEF

Congestion is defined as the overflow of routing demand over available routing resource in the routing stage of the back-end design. It is frequently adopted as the metric to evaluate routability, i.e., the prospective quality of routing based on the current design solution. The congestion prediction is necessary to guide the optimization in placement stage and reduce total turn-around time.

The network of `Global Placement with Deep Learning-Enabled Explicit Routability Optimization` [1] uses an FCN based encoder-decoder architecture to translate the image-like features into a congestion map. The architecture is shown in Fig 1.




```
class conv(nn.Module):
    def __init__(self, dim_in, dim_out, kernel_size=3, stride=1, padding=1, bias=True):
        super(conv, self).__init__()
        self.main = nn.Sequential(
            nn.Conv2d(dim_in, dim_out, kernel_size=kernel_size, stride=stride, padding=pad
            nn.InstanceNorm2d(dim_out, affine=True),
            nn.LeakyReLU(0.2, inplace=True),
            nn.Conv2d(dim_out, dim_out, kernel_size=kernel_size, stride=stride, padding=pa
            nn.InstanceNorm2d(dim_out, affine=True),
            nn.LeakyReLU(0.2, inplace=True),
        )
```

Tutorial & documentation

https://circuitnet.github.io/

Research & Contests using CircuitNet

[NVIDIA, arXiv'24]

Optimizing Predictive AI in Physical Design Flows with Mini Pixel Batch Gradient Descent

Haoyu Yang, NVIDIA Corp.
Anthony Agnesina, NVIDIA Corp.
Haoxing Ren, NVIDIA Corp.

[HUST, NeurIPS'24]

Circuit as Set of Points

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[1]School of EIC, Huazhong University of Science and Technology
[2]Horizon Robotics

[UCSD, arXiv'24]

On Robustness and Generalization of ML-Based Congestion Predictors to Valid and Imperceptible Perturbations

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EDA Elite Contest 2023 for IR Drop Prediction

2023 Integrated Circuit EDA Elite Challenge

Problem Guide

https://eda.icisc.cn/en/

一、 **赛题名称**：基于机器学习的 SoC 电源网络静态压降预测

Contest Question : Machine Learning driven Static IR drop estimation of SoC power grid network

二、 **命题企业**：杭州行芯科技有限公司

Question provider: Hangzhou Phlexing Technology Co., Ltd. (Phlexing)

CCF-Chip Contest 2024 for DRC Prediction

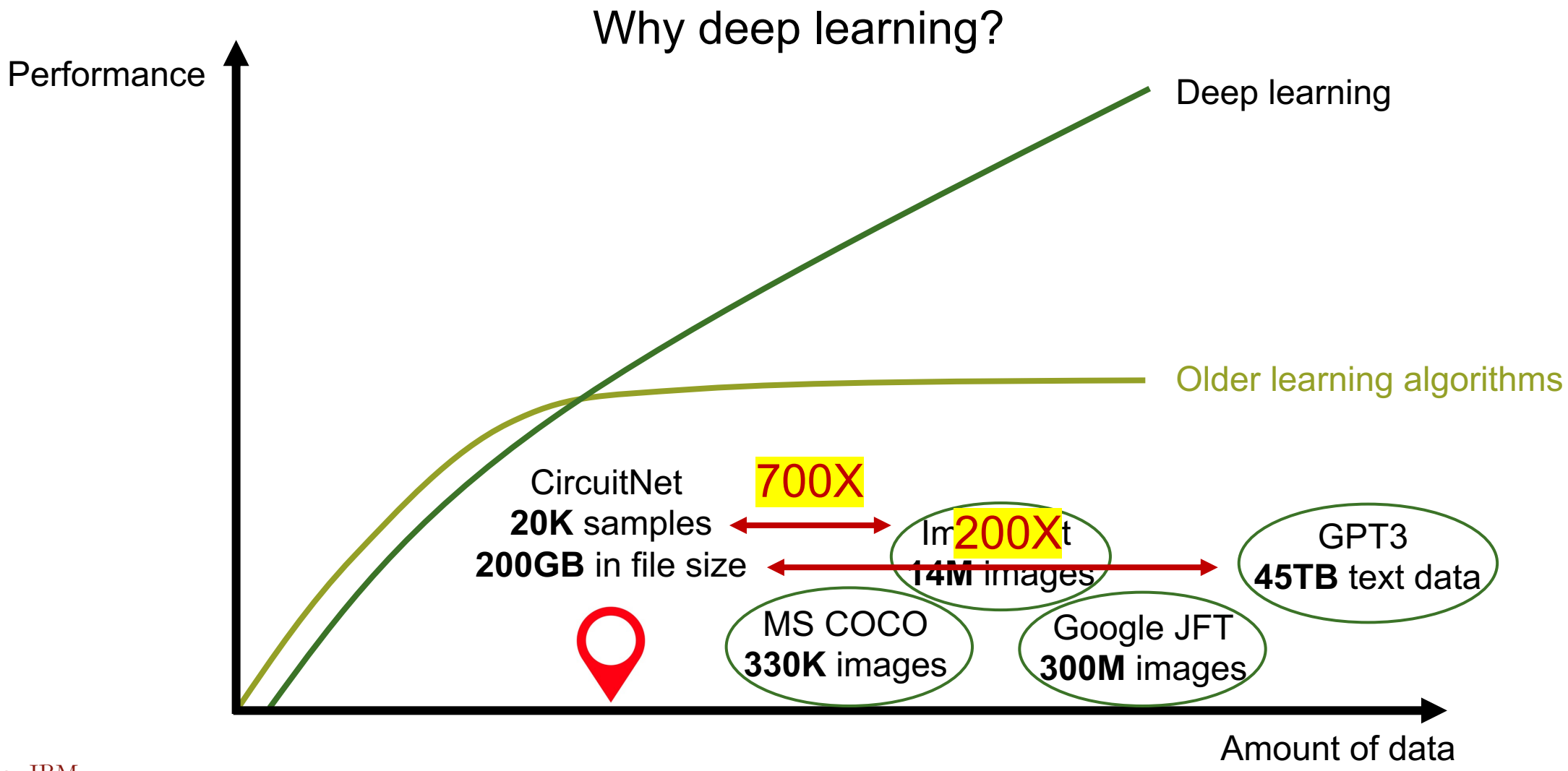
ASIC DRC违例预测模型设计及AI-PC部署挑战赛

https://ccf.org.cn/chip2024

赛题背景

随着人工智能和大数据应用的不断发展，对于高性能、低功耗的ASIC（专用集成电路）芯片需求日益增长。然而，设计和验证ASIC芯片的过程中，面临着一个重要的挑战：设计规则检查（DRC）违例的预测和解决。DRC是芯片设计流程中的关键步骤之一，用于确保芯片布局和连线满足制造工艺的要求。DRC规则由芯片制造工艺厂商提供，通常包括关于金属线间距、晶体管尺寸等方面的规定。设计人员必须确保他们的设计不会违反这些规则，否则可能导致芯片生产失败或性能下降。

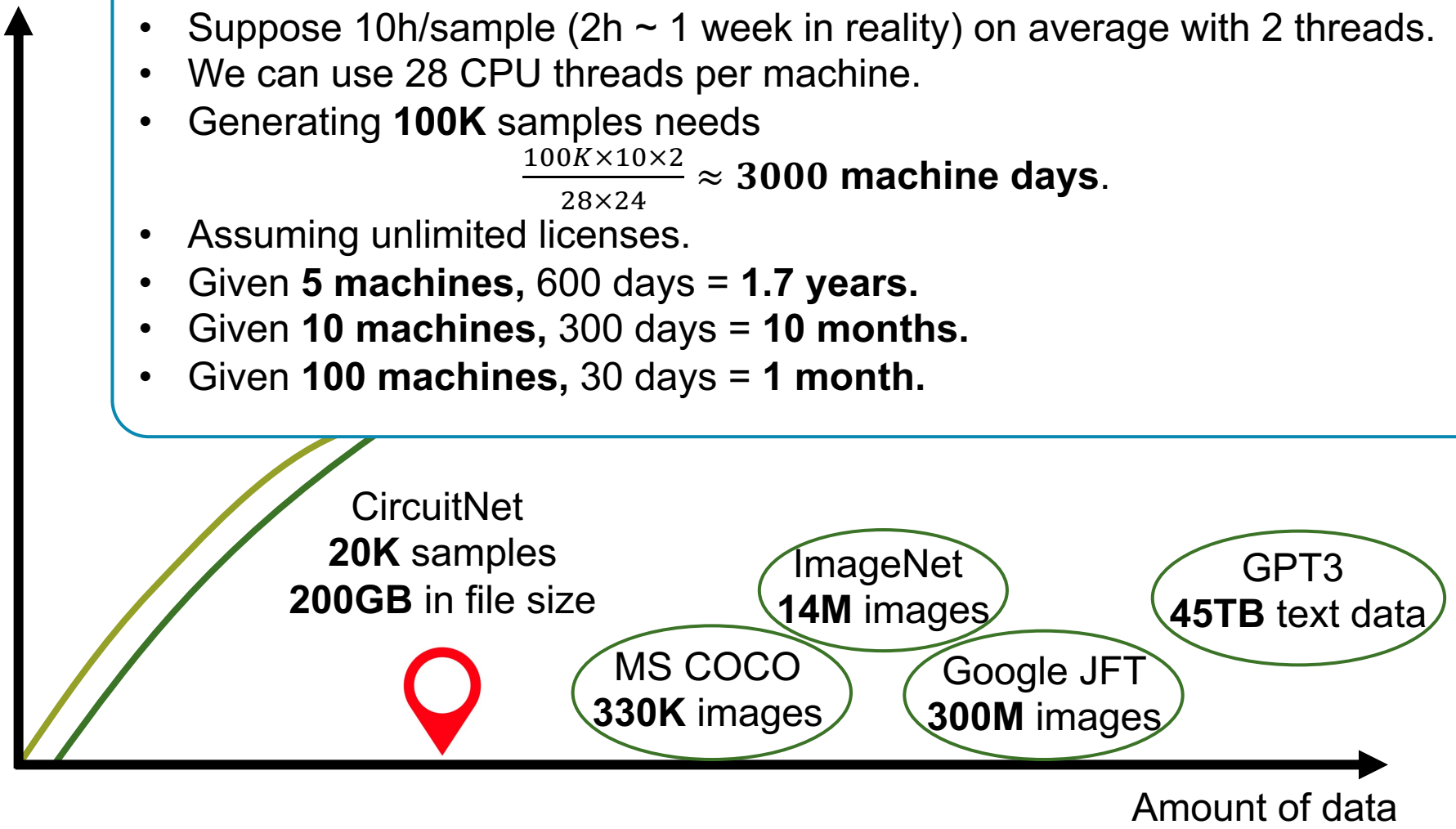
Where are We and Where to Go



Curtesy IBM

Where are We and Where to Go

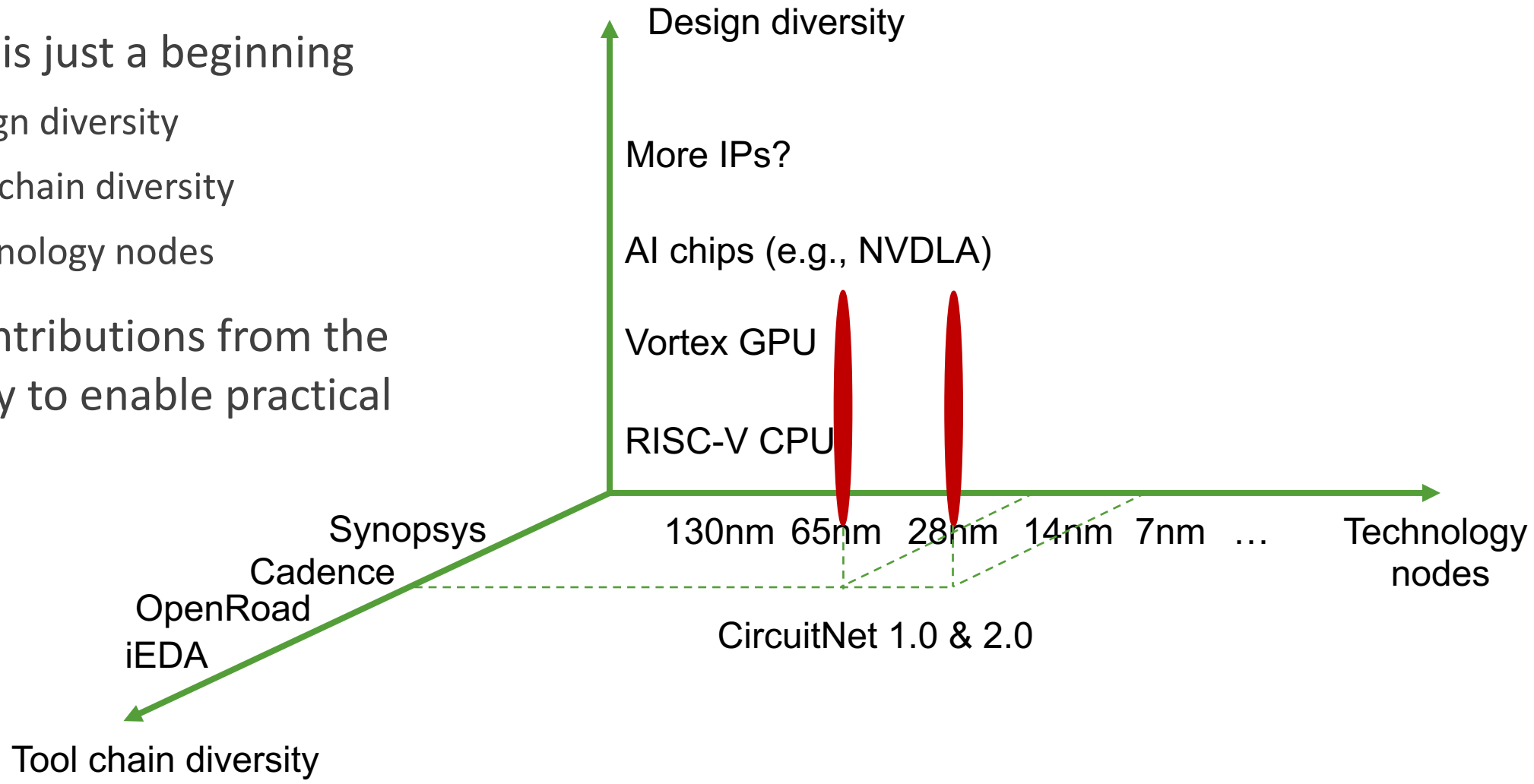
- Suppose 10h/sample (2h ~ 1 week in reality) on average with 2 threads.
- We can use 28 CPU threads per machine.
- Generating **100K** samples needs $\frac{100K \times 10 \times 2}{28 \times 24} \approx$ **3000 machine days**.
- Assuming unlimited licenses.
- Given **5 machines,** 600 days = **1.7 years.**
- Given **10 machines,** 300 days = **10 months.**
- Given **100 machines,** 30 days = **1 month.**



Curtesy IBM

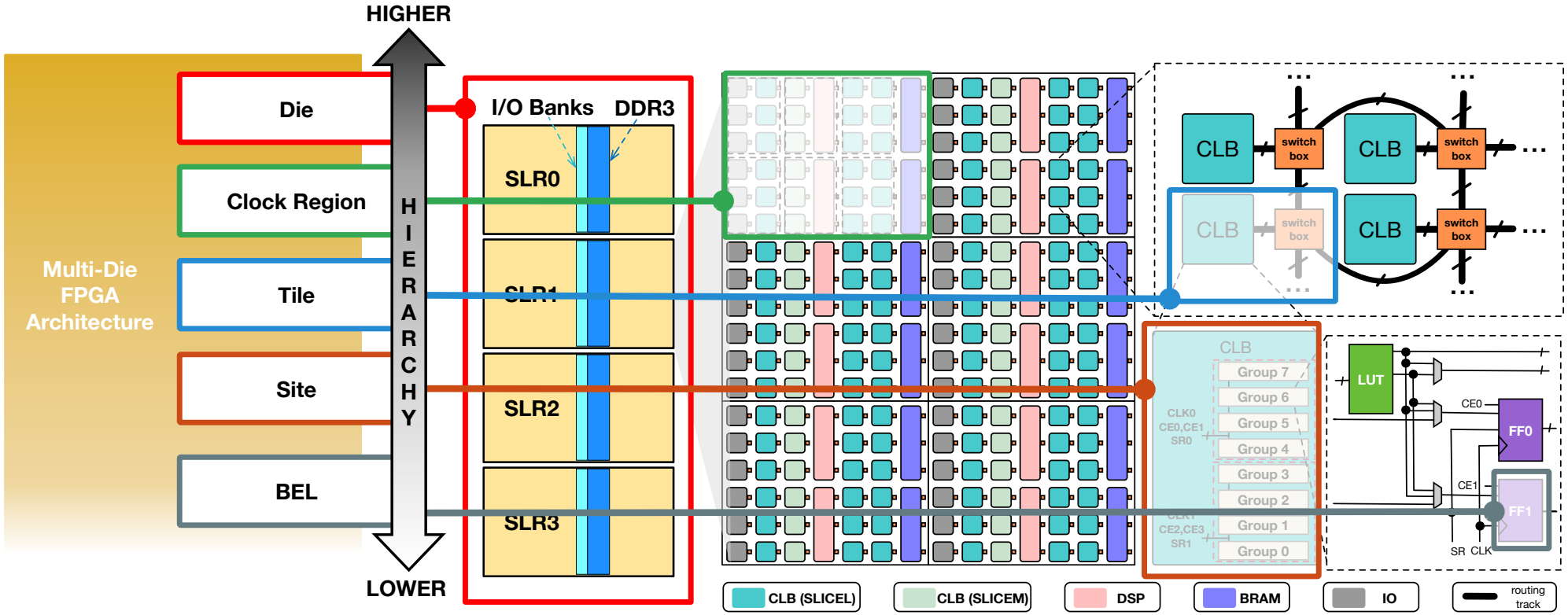
Call for Contributions

- Dataset is critical to AI for EDA
- CircuitNet is just a beginning
  - More design diversity
  - More tool chain diversity
  - More technology nodes
- Call for contributions from the community to enable practical AI for EDA



OpenPARF: P&R for FPGA [DAC'22, ASPDAC'23, ASICON'23, TCAS-I'23]

- 2.5D multi-die heterogeneous FPGA architecture
  - Industrial architecture for placement and routing
  - Competitive performance with nonlinear placement optimization and parallel routing flow
  - https://github.com/PKU-IDEA/OpenPARF



Thanks!

Questions are Welcome

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