iEDA: An Open-source EDA Infrastructure and Toolchain

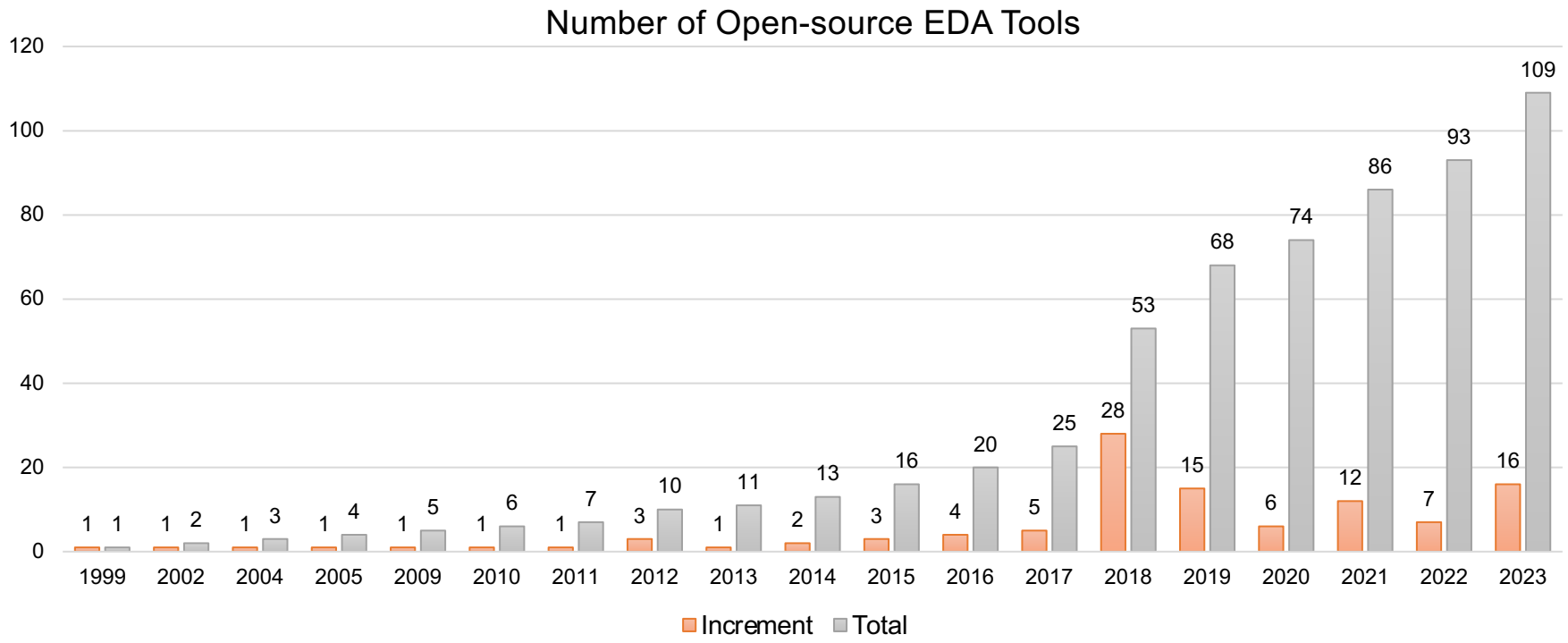
Xingquan Li

iEDA Community

Speaker: Zhizheng Zeng

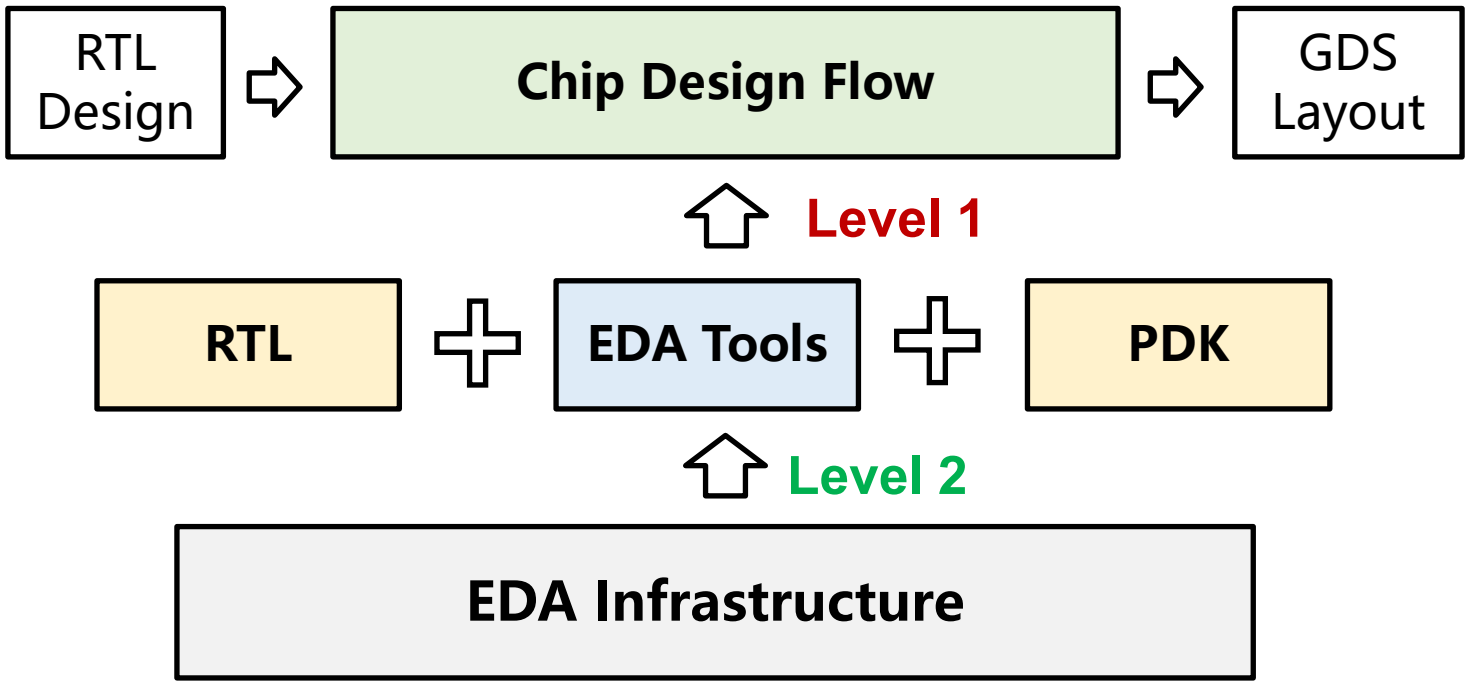
Increasing Open-souce EDA Tools

- Open-souce in EDA may be a tendency



We Need Infrastructure

- **Level 1:** Open-source tools, RTLs, PDKs support chip design
- **Level 2:** Open-source Infrastructure supports EDA development



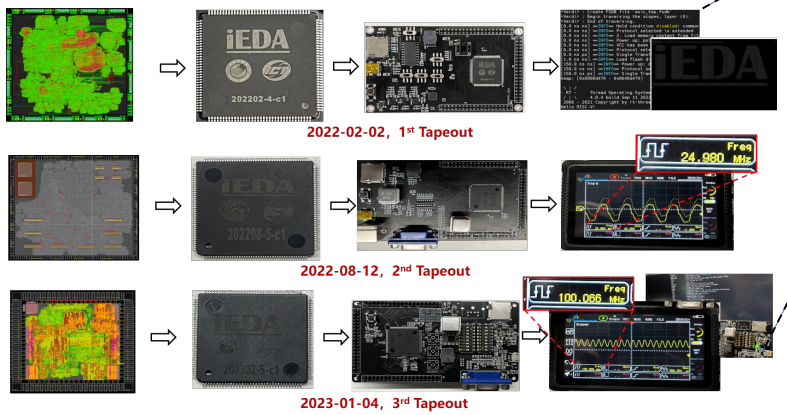
iEDA Overview

- **EDA Infrastructure、EDA Tools、3 times tape-out design by iEDA**
  - **Level 1: Open-source EDA, RTL, PDK, supporting chip design;**
  - **Level 2: Open-source Infrastructure supports EDA development and research**

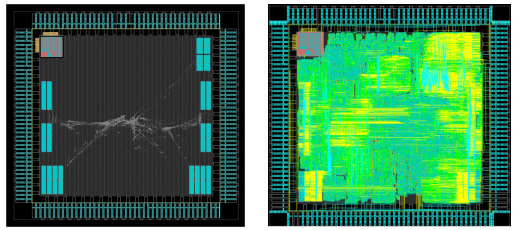
1st Tapeout
- **RTL**: ysyx03
- **PDK**: 110nm
- **Area**: 3mm × 3.5 mm
- **Power**: dynamic = 48mW, leakage = 7 mW
- **Freq.**: 25MHz
- **Scale**: >70万 Gates
- **Features**: 5 pipeline, Chiplink, UART、SPI、PCB clock, support RT-thread

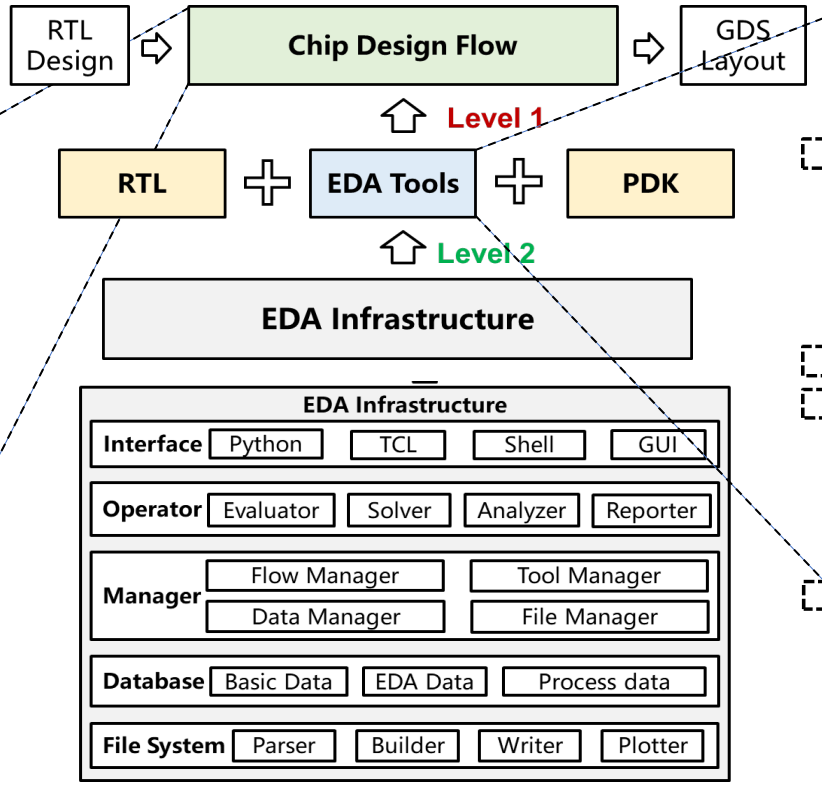
2nd Tapeout
- **RTL**: ysyx04
- **PDK**: 110nm
- **Area**: 4.5mm × 4.5 mm
- **Power**: dynamic = 343mW, leakage = 21 mW
- **Freq.**: 25MHz
- **Scale**: >1.5M Gates
- **Features**: 11 pipelines with cache, IP: UART、VGA、PS/2、SPI、SDRAM、2 PLLs, support Linux

3rd Tapeout
- **RTL**: ysyx04
- **PDK**: 28nm
- **Area**: 1.5mm × 1.5 mm
- **Power**: dynamic = 317mW, leakage = 29 mW
- **Freq.**: 200MHz
- **Scale**: >1.5M Gates
- **Features**: 11 pipelines with cache, IP: UART、VGA、PS/2、SPI、SDRAM、2 PLLs, support Linux

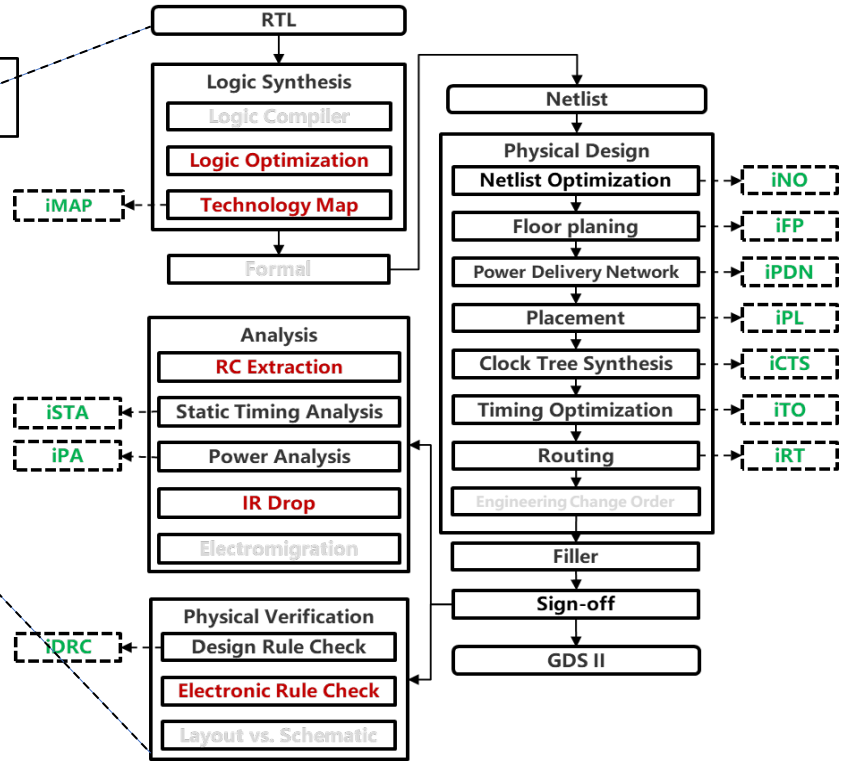


3 times tape-out





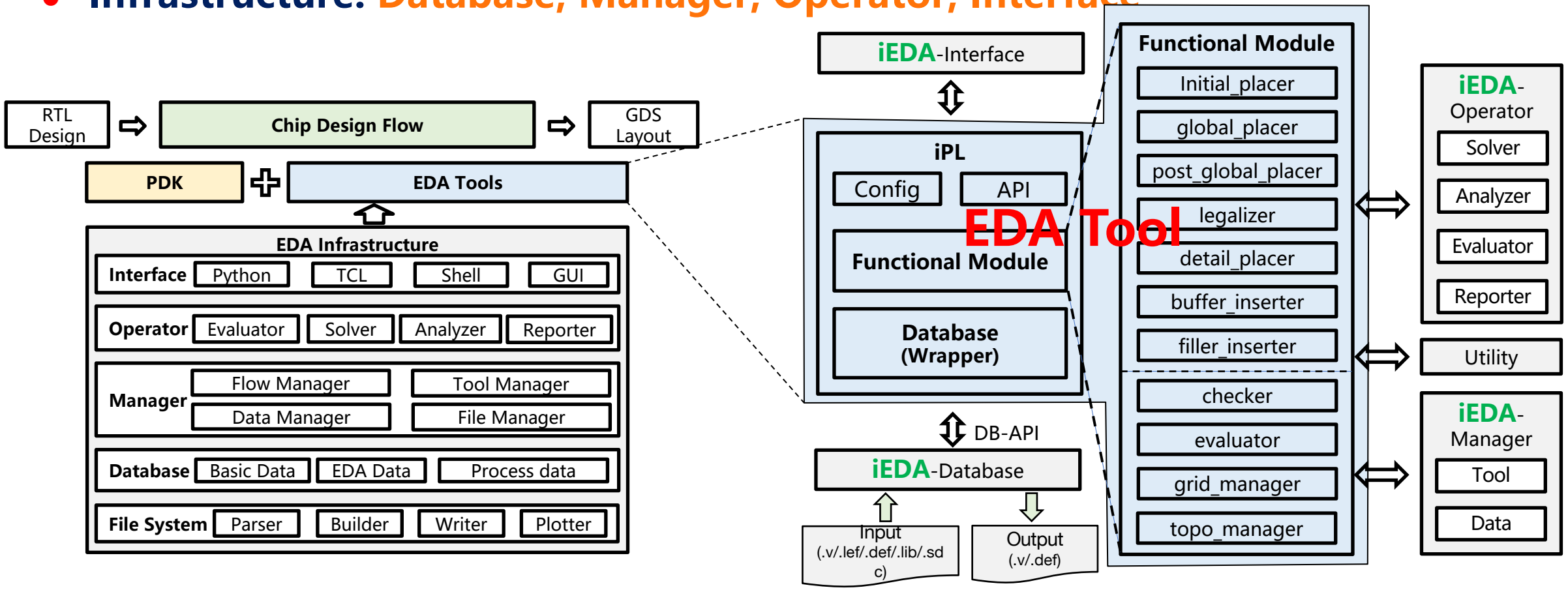
1 EDA infrastructure



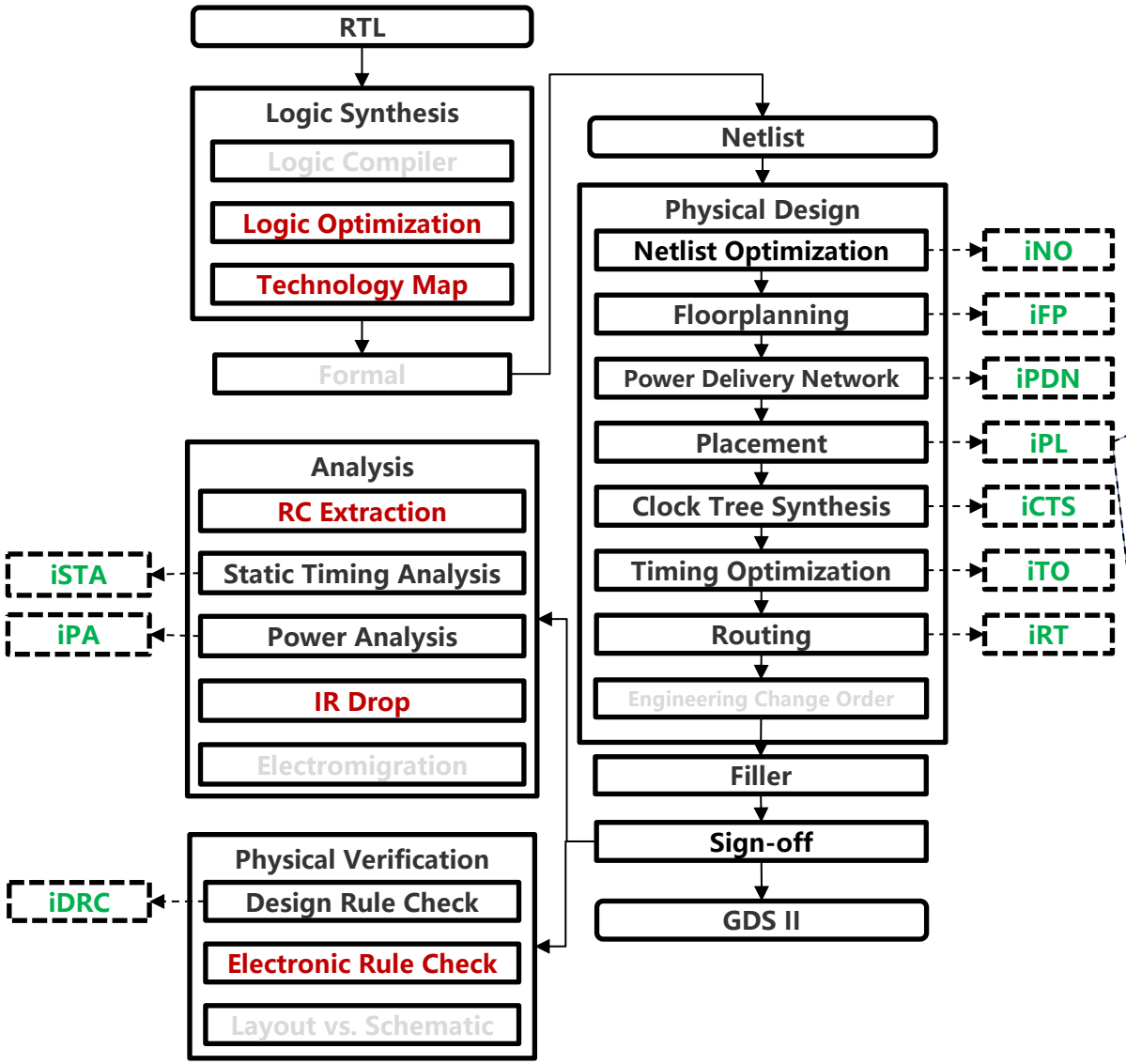
11 EDA tools, 200 technologies, 300 K lines codes

iEDA: Infrastructure

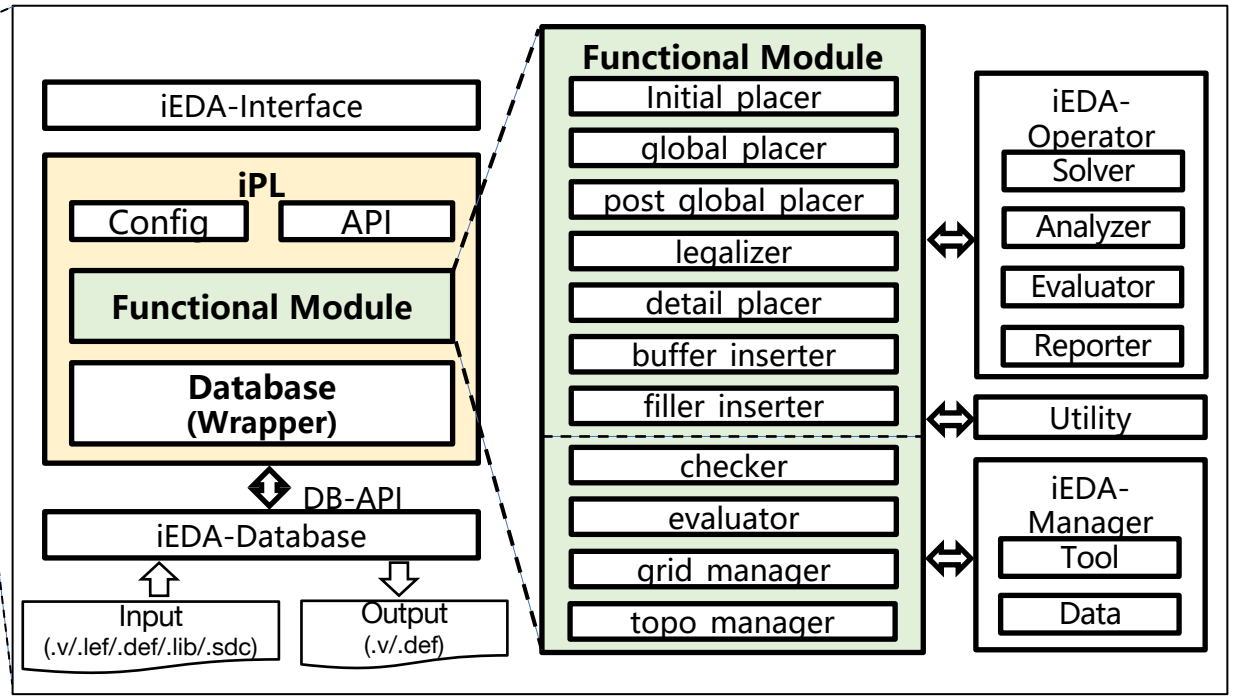
- To fast develop high-quality EDA tool, we need a **S**oftware **D**evelopment **K**it (**SDK**)
- iEDA can be used to support developing EDA tool or algorithm
- **Infrastructure: Database, Manager, Operator, Interface**



iPD: Physical Design Toolchain

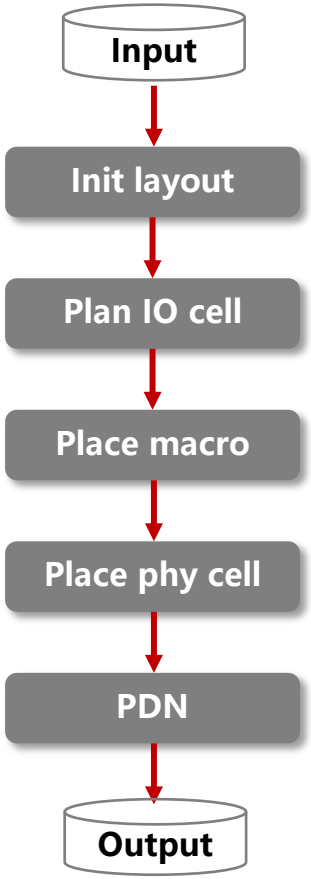


- **Netlist-to-GDS II**
  - **11 tools, and other 5 tools are R&Ding.**
  - **Design, Analysis, Verification**
- **Design Concept:**
  - **Unified framework, deconstructed and merged**
  - **multi-lingual interface, hot-pluggable modules.**

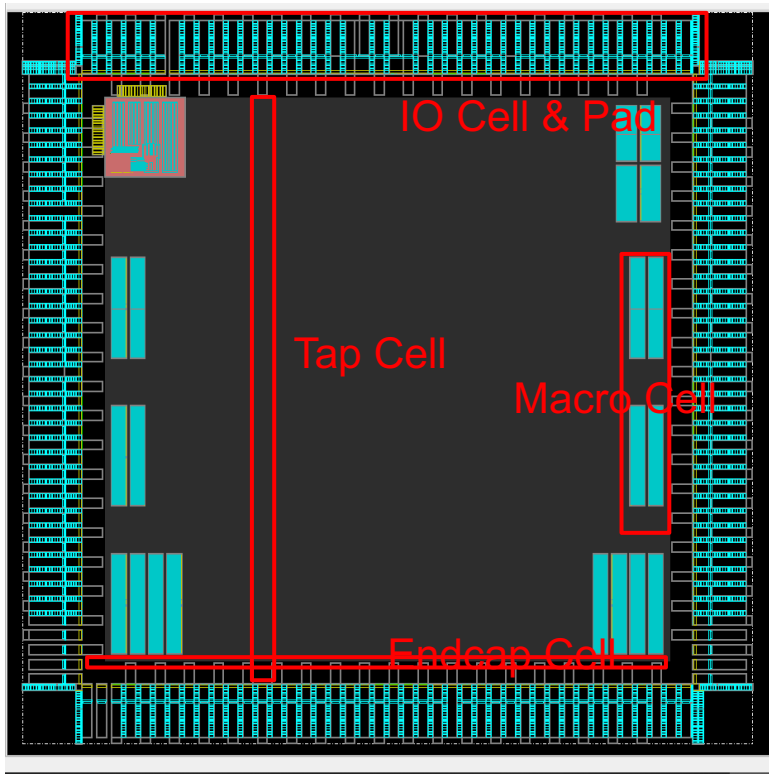


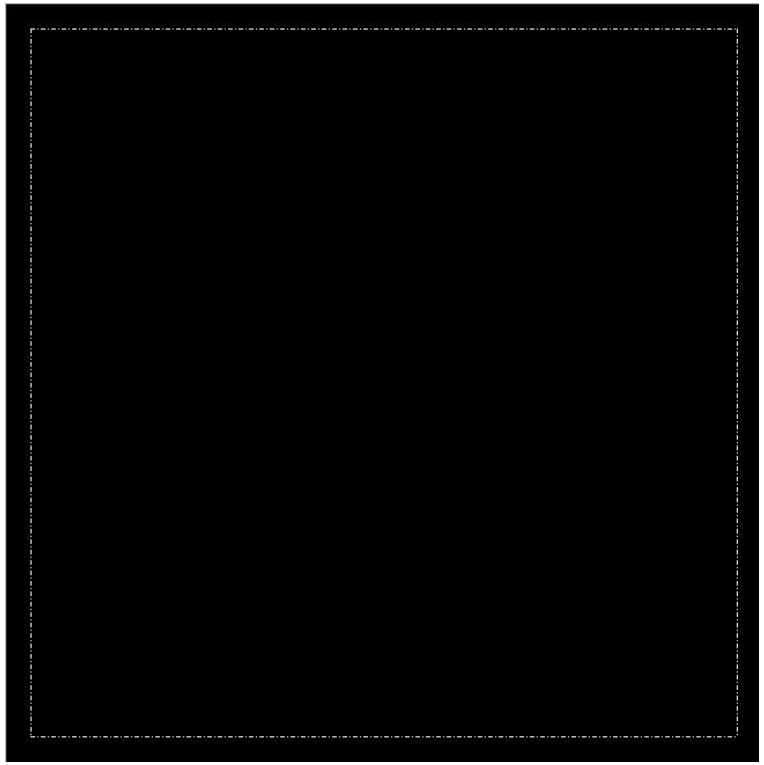
Floorplan (iFP) & Power Delivery Network (iPDN)

Flow



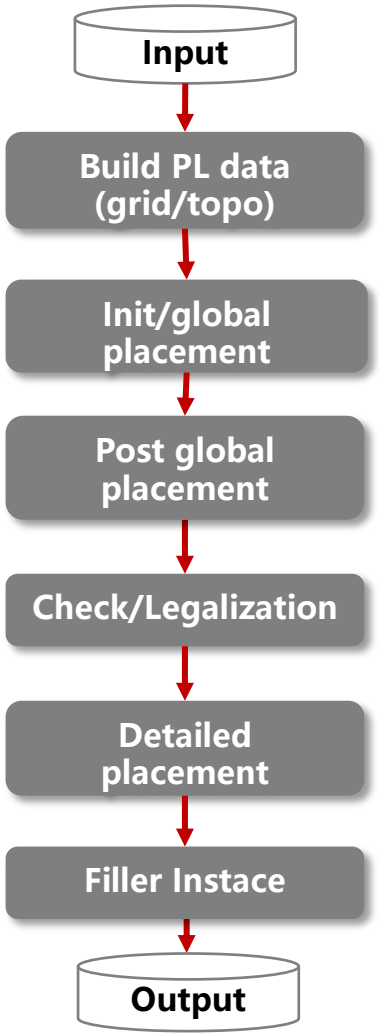
Key Metrics	Data
DIE Area	1.5 × 1.5 mm^2
DIE Utili	0.166554
Core Area	1.16 × 1.15 cm^2
Core Utili	0.279541
#IO Pin	110
#Instance	297504
#Net	311869
Pin	**pin（>= 32）= 2893**
PDN	M1、M2、M7、M8、M9、AP

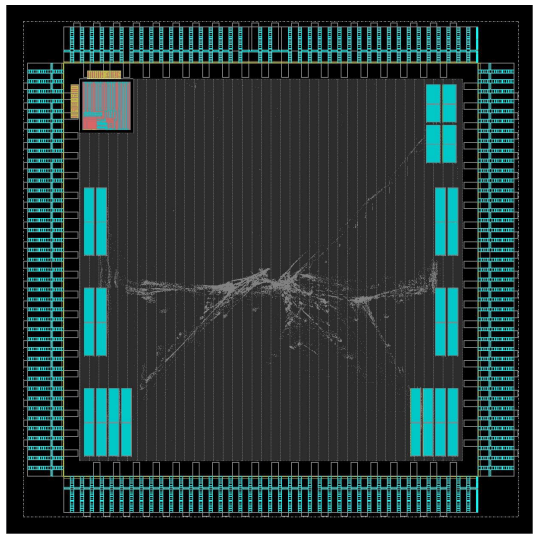




Placement (iPL)

Flow





Basic Summary

```
summary_report.txt
scripts > sky130 > result > pl > report > summary_report.txt
1   Generate the report at 2023-08-15T15:10:33
2   +-------------------------+----------+
3   | Base Info               | Value    |
4   +-------------------------+----------+
5   | Design                  | gcd      |
6   | Utilization             | 0.098599 |
7   | Site Num                | 78 * 542 |
8   | Instances Count         | 795      |
9   |  - Macro Count          | 0        |
10  |  - StdCell Count        | 795      |
11  |  -- FlipFlop Count      | 34       |
12  |  -- Clock Buffer Count  | 0        |
13  |  -- Normal Logic Count  | 761      |
14  | Nets Count              | 675      |
15  |  - Signal Net Count     | 674      |
16  |  - Clock Net Count      | 1        |
17  |  - Reset Net Count      | 0        |
18  |  - Other Net Count      | 0        |
19  +-------------------------+----------+
20
21  +-----------------------------------+-----------+
22  | Violation Info                    | Value     |
23  +-----------------------------------+-----------+
24  | Core Range Violated Count         | 0         |
25  | Row/Site Alignment Violated Count | 0         |
26  | Power Alignment Violated Count    | 0         |
27  | Overlap Violated Count            | 0         |
28  +-----------------------------------+-----------+
29
30  +-----------------------------------+-----------+
31  | Wirelength Info                   | Value     |
32  +-----------------------------------+-----------+
33  | Total HPWL                        | 14402289  |
34  | Max HPWL                          | 328905    |
35  | Total STWL                        | 15057480  |
36  | Max STWL                          | 512025    |
37  | LongNet HPWL (Exceed 1000000) Count | 0       |
38  +-----------------------------------+-----------+
39
40  +-------------------+-----------+
41  | Bin Density Info  | Value     |
42  +-------------------+-----------+
43  | Peak BinDensity   | 1.000000  |
44  +-------------------+-----------+
45
46  +-------------------+-----------+-----------+-----------+-----------+
47  | Clock Timing Info | Early WNS | Early TNS | Late WNS  | Late TNS  |
48  +-------------------+-----------+-----------+-----------+-----------+
49  | core_clock        | 0.000000  | 0.000000  | -0.194720 | -2.818471 |
50  +-------------------+-----------+-----------+-----------+-----------+
51
52  +-----------------------------------+-----------+
53  | Congestion Info                   |           |
54  +-----------------------------------+-----------+
55  | Average Congestion of Edges       | 0.537355  |
56  | Total Overflow                    | 53.000000 |
57  | Maximal Overflow                  | 18.000000 |
58  +-----------------------------------+-----------+
```

Wirelength
wl_detail_report.txt

Instance density

Timing

Congestion

Design rule violation
violation_detail_report.txt

■ Min Wirelength Model

$$\min_{\boldsymbol{v}} \quad W(\boldsymbol{v})$$
$$s.t. \quad \rho_b(\boldsymbol{v}) \le \rho_0, \qquad \forall b \in B$$

where v is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density thredhold.

$\boldsymbol{W(v)}$

$$HPWL_{ex}(\mathbf{v}) = \max_{i,j \in e} |x_i - x_j|$$

$$LSE_{ex} = \gamma \left(\ln \left(\sum_{i \in e} \exp\left(\frac{x_i}{\gamma} \right) \right) + \ln \left(\sum_{i \in e} \exp\left(\frac{-x_i}{\gamma} \right) \right) \right)$$

$\boldsymbol{\rho_b(v)}$

$$D(\boldsymbol{v}) = \frac{1}{2} \sum_{v \in V} D_i(x,y) = \frac{1}{2} \sum_{v \in V} q_i \psi_i(x,y)$$

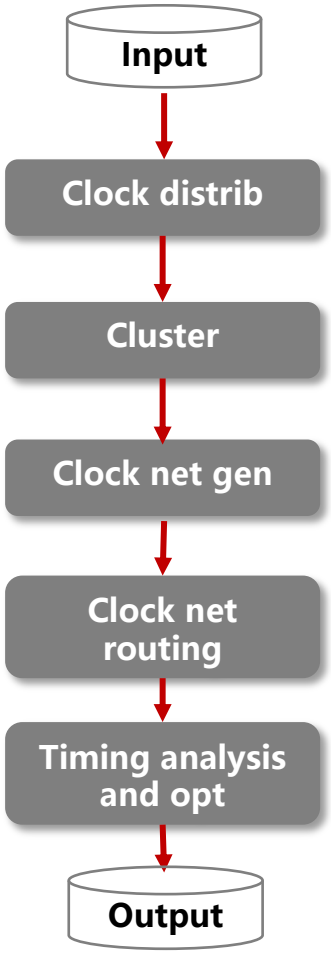
$$\begin{cases} \nabla \cdot \nabla \psi(x,y) = -\rho(x,y), \\ \hat{\boldsymbol{n}} \cdot \psi(x,y) = \mathbf{0}, \qquad (x,y) \in \partial R \\ \iint_R \rho(x,y) = \iint_R \psi(x,y) = 0. \end{cases}$$

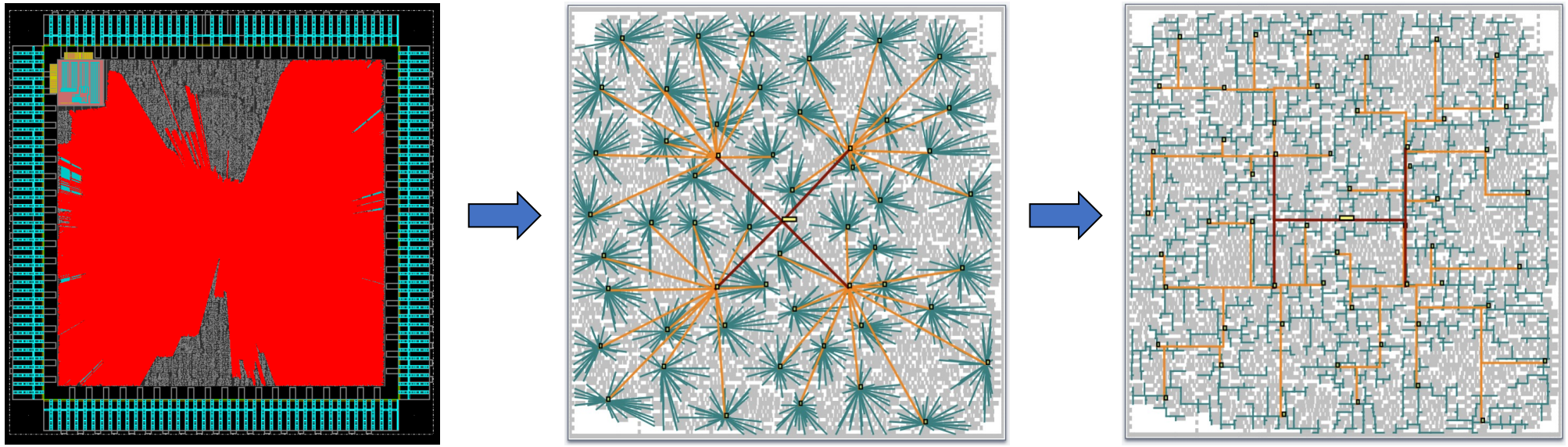
$$\min_{\boldsymbol{v}} \quad f(v) = W(\boldsymbol{v}) + \lambda \sum_{\forall b \in B} \boldsymbol{\rho_b}(\boldsymbol{v})$$

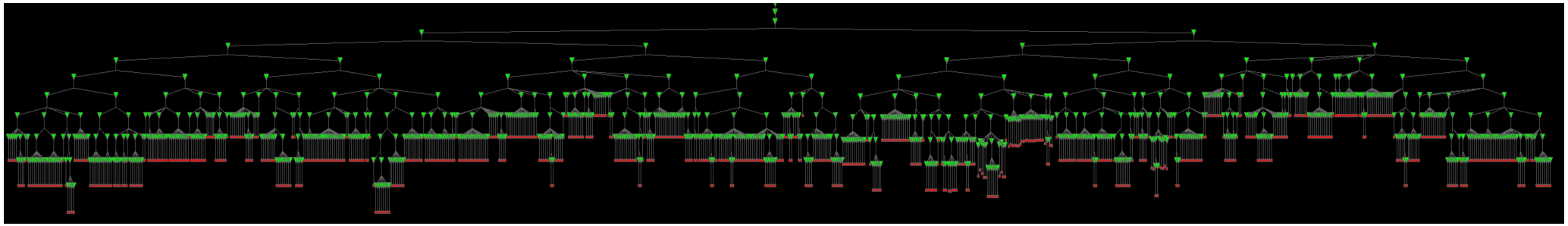
- **Nesterov Method or** Conjugate Gradient

Clock Tree Synthesis (iCTS)

Flow







Timing

- Latency (max delay)
- Skew

Power

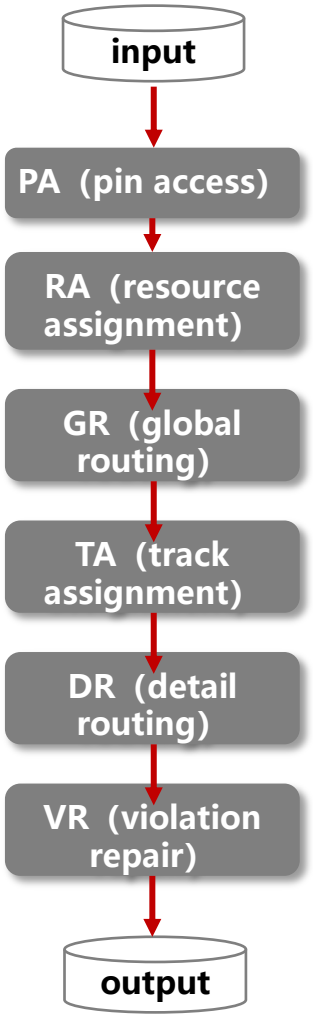
- Buffering
- Wirelength

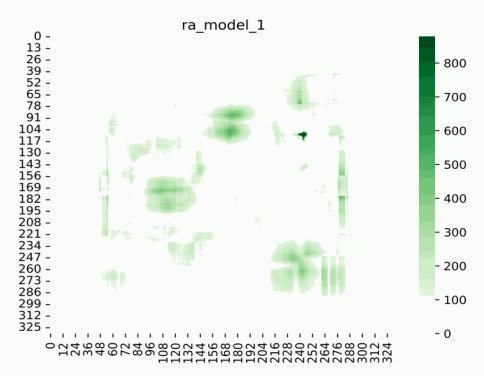
Violation

- Fanout
- Capacitance
- Slew (transition)

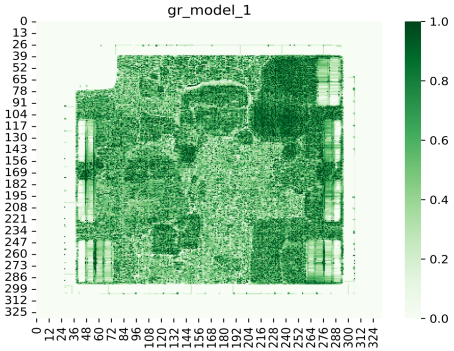
Routing (iRT)

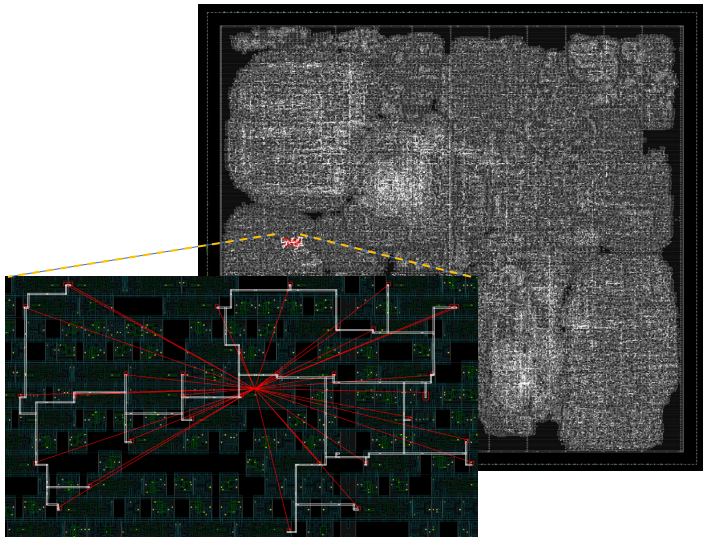
Flow



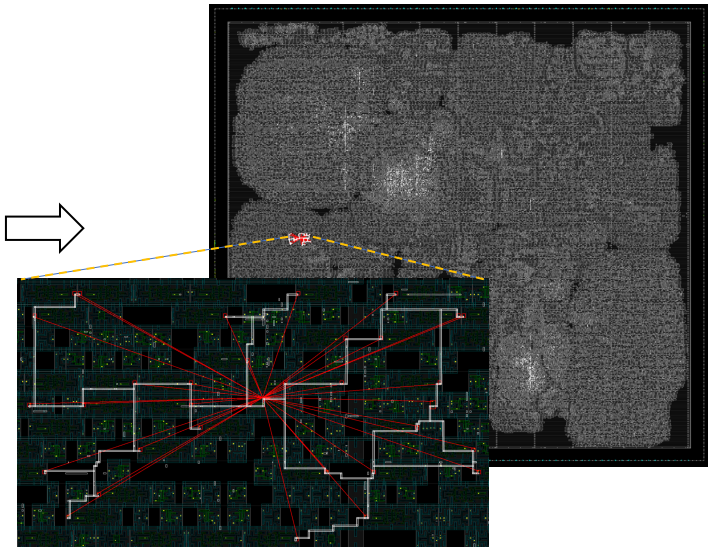


Layout resource/congestion





first iteration routing result



final routing result

Access Type	Pin Number
Track Grid	876856(75.2479%)
On Track	259825(22.297%)
On Shape	28608(2.45501%)
Total	1165289

Routing Layer	Port Number	Access Point Number
M1	806086(68.3279%)	799044(68.5705%)
M2	366214(31.0422%)	362248(31.0865%)
M3	7073(0.599543%)	3997(0.343005%)
M4	358(0.0303459%)	0(0%)
M5	0(0%)	0(0%)
M6	0(0%)	0(0%)
M7	0(0%)	0(0%)
M8	0(0%)	0(0%)
M9	0(0%)	0(0%)
AP	0(0%)	0(0%)
Total	1179731	1165289

Pin Access

Routing Layer	Wire Length / um
M1	9774(0.117785%)
M2	846292(10.1985%)
M3	1.98405e+06(23.9095%)
M4	1.78748e+06(21.5406%)
M5	1.29642e+06(15.6229%)
M6	1.41202e+06(17.016%)
M7	960890(11.5795%)
M8	539.92(0.00650648%)
M9	720(0.00867659%)
AP	0(0%)
Total	8.29819e+06

Cut Layer	Via Number
CO	0(0%)
VIA1	595417(30.6475%)
VIA2	682833(35.147%)
VIA3	400386(20.6088%)
VIA4	135600(6.97965%)
VIA5	89437(4.60353%)
VIA6	38709(1.99244%)
VIA7	262(0.0134857%)
VIA8	148(0.0076179%)
RV	0(0%)
Total	1942792

Resource Overflow	GCell Number
[0,0.1)	921387(83.1%)
[0.1,0.2)	57544(5.19%)
[0.2,0.3)	51492(4.64%)
[0.3,0.4)	40084(3.61%)
[0.4,0.5)	21944(1.98%)
[0.5,0.6)	10780(0.972%)
[0.6,0.7)	4140(0.373%)
[0.7,0.8)	1223(0.11%)
[0.8,0.9)	222(0.02%)
[0.9,1]	74(0.00667%)
Total	1108890

Access Overflow	GCell Number
[0,0.1)	1.78338e+06(80.4%)
[0.1,0.2)	108739(4.9%)
[0.2,0.3)	79939(3.6%)
[0.3,0.4)	90020(4.06%)
[0.4,0.5)	56112(2.53%)
[0.5,0.6)	36741(1.66%)
[0.6,0.7)	30046(1.35%)
[0.7,0.8)	12155(0.548%)
[0.8,0.9)	8771(0.395%)
[0.9,1]	11881(0.536%)
Total	2217780

Wirelength and via

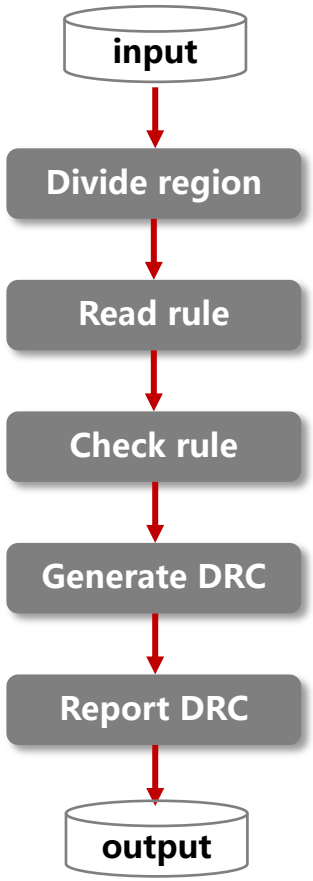
Drc Summary

DRC Type	Number
Cut Different Layer Spacing	433141
Cut EOL Spacing	197803
Cut Enclosure	152168
Cut EnclosureEdge	0
Cut Spacing	358281
Metal Corner Filling Spacing	10443
Metal EOL Spacing	869415
Metal JogToJog Spacing	0
Metal Notch Spacing	733497
Metal Parallel Run Length Spacing	864355
Metal Short	1745445
MinHole	1260
MinStep	670823
Minimal Area	1248072

Design rule check

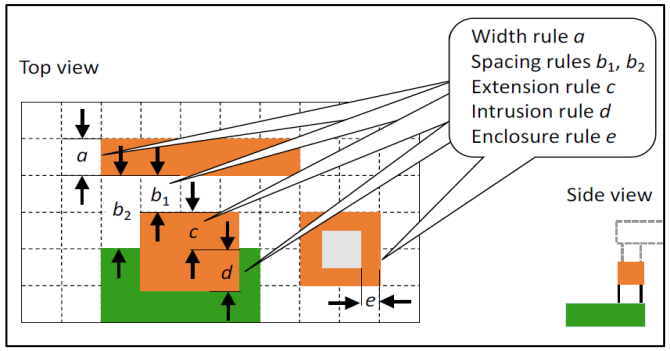
Design Rule Check (iDRC)

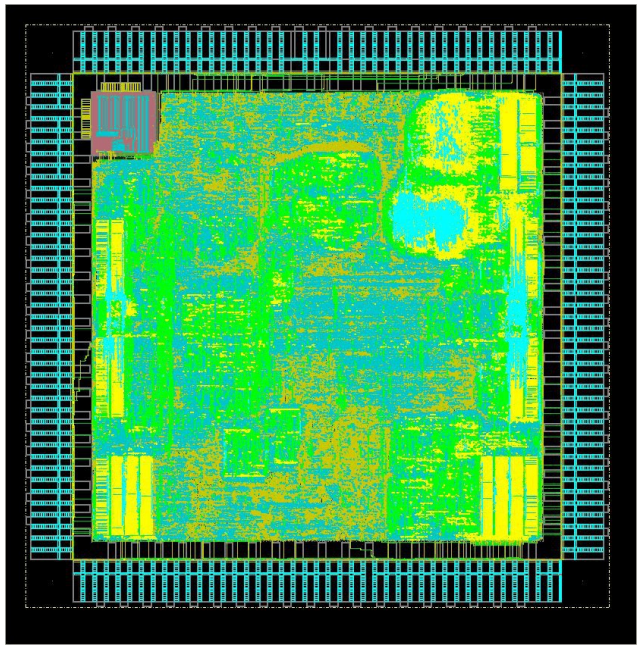
Flow

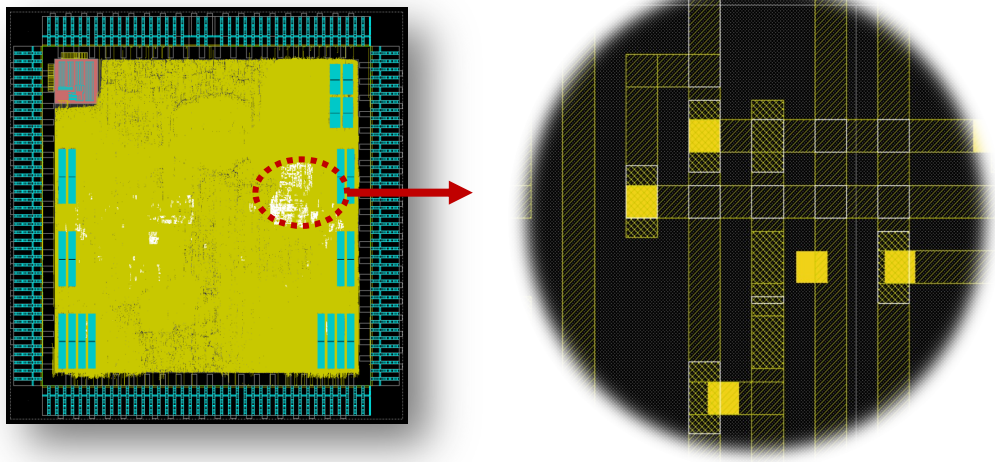


Support DRC Rules:

- Cut Different Layer Spacing
- Cut EOL Spacing
- Cut Enclosure
- Cut Enclosure Edge
- Cut Spacing
- Metal Corner Filling Spacing
- Metal EOL Spacing
- Metal JogToJog Spacing
- Metal Notch Spacing
- Metal Parallel Run Length Spacing
- Metal Short
- MinHole
- MinStep
- Minimal Area



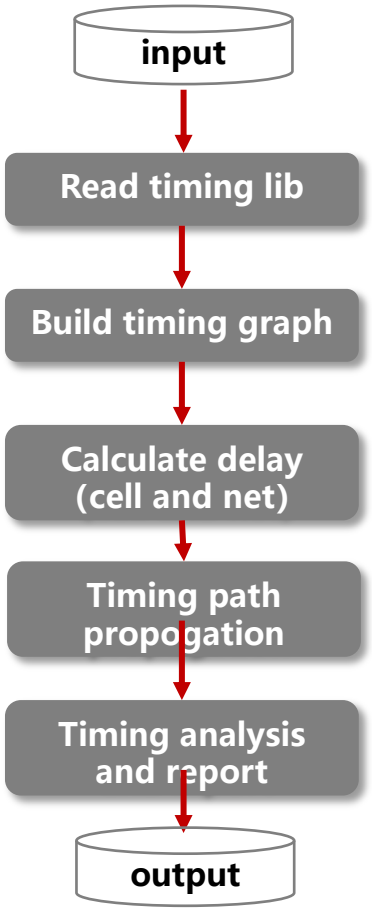




DRC Visulization

Static Timing Analysis (iSTA)

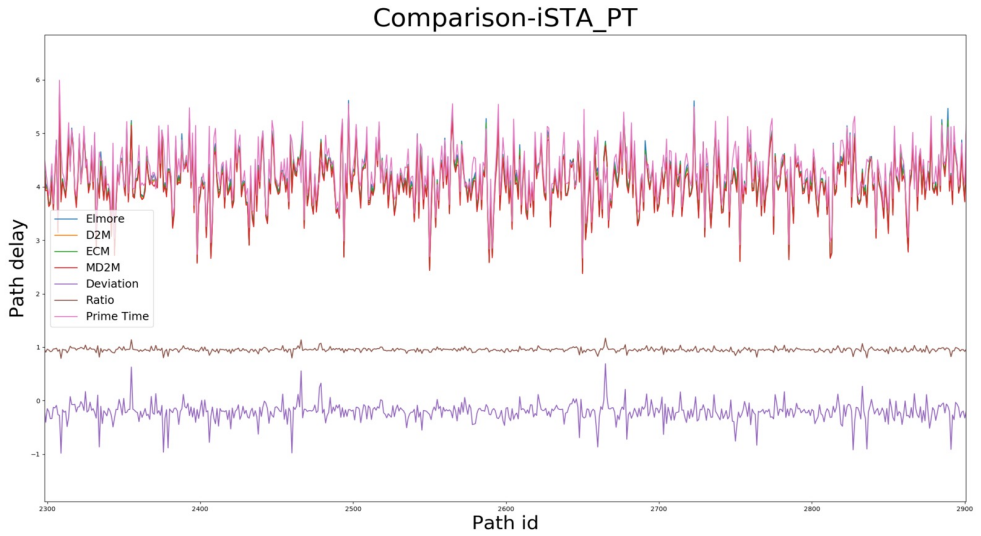
FLow



Feature

Feature
Support hierarchy netlist and def
Basic setup/hold analysis
Support NLDM/Elmore
Support CCS model
Support high-level net delay model
Support sdf mark
OCV
AOCV
POCV
Consider IRDrop analysis on multi-voltage domain
Hierarchy analysis
Crosstalk analysis
clock gate analysis
Latch analysis

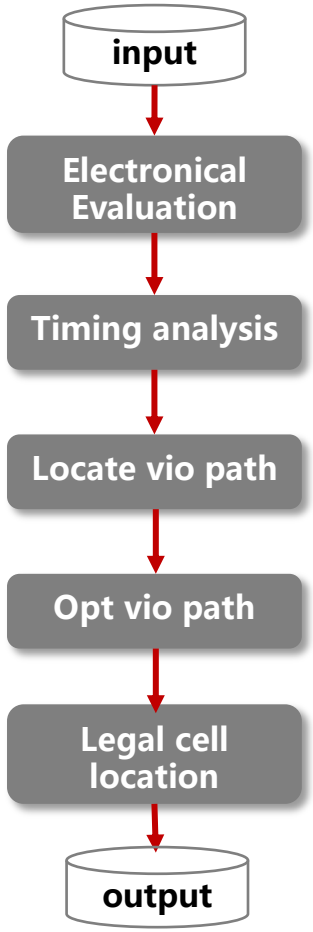
Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		0.885	0.011	0.011r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.011r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		0.885	0.032	0.043r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.043r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		0.885	0.021	0.064r
u0_rcg/mux_core_clk_0 (clock net)	17				0.000			
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.064	0.064
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
u0_rcg/mux_core_clk_div3/gt_en1_reg:Q (DFSNQD1BWP40P140LVT)		0.001	0.000	0.009		0.820	0.045	0.109r
u0_rcg/mux_core_clk_div3/gt_en1 (net)	1				0.000			
u0_rcg/mux_core_clk_div3/U_GT1:E (CKLNQD4BWP40P140LVT)		0.001	0.000	0.009		1.000	0.000	0.109r
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		1.039	0.013	0.013r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.013r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		1.039	0.038	0.051r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.051r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		1.039	0.025	0.076r
u0_rcg/mux_core_clk_0 (clock net)	17				NA			
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)		0.001	0.000	0.000		1.000	0.000	0.076r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.076	0.076
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)								r
library hold time							0.000	0.076
clock reconvergence pessimism						-0.011	0.064	
data require time								0.064
data arrival time								0.109
slack (MET)								0.045



pt/ista ratio	value
mean	1.11
variance	0.00095
median	1.107
maximum	1.5404
minimum	0.9035

Timing Optimization (iTO)

Flow



Key parameter config	
Input	iPL.def, iCTS.def
output	iTO_setup_result.def, iTO_hold_reslut.def
setup_slack_margin	setup slack value
hold_slack_margin	hold slack value
max_buffer_percent	Area ratio of inserted buffer
max_utilization	Core utilization
DRV_insert_buffers	Available buffer for optimizing DRV
setup_insert_buffers	Available buffer for optimizing setup
hold_insert_buffers	Available buffer for optimizing hold
number_passes_allowed_decreasing_slack	The number of times that WNS is allowed continuously decrease when opt setup
rebuffer_max_fanout	For setup, a wire network is not optimized for buffer insertion when its fanout exceeds this value
split_load_min_fanout	For setup, fanout is reduced by inserting a buffer when fanout is greater than this value

DRV report

```
path
Worst Slack: -5.88383
Found 3 slew violations.
Found 11 capacitance violations.
Found 0 fanout violations.
Found 0 long wires.
Before ViolationFix | slew_vio: 3 cap_vio: 11 fanout_vio: 0 length_vio: 0
The 1th check
After ViolationFix | slew_vio: 3 cap_vio: 0 fanout_vio: 0 length_vio: 0
The 2th check
After ViolationFix | slew_vio: 0 cap_vio: 0 fanout_vio: 0 length_vio: 0
DRV_net_3
Inserted 11 buffers in 12 nets.
Resized 0 instances.
```

Setup report

```
Inserted 10 hold buffers.

Worst Hold Path Launch : u0_soc_top/u0_sdram_axi/u_core/sample_data0_q_reg_8_:CP
Worst Hold Path Capture: u0_soc_top/u0_sdram_axi/u_core/sample_data_q_reg_8_:CP

The 1-th timing check.
    worst hold slack: -1.28225
Unable to repair all hold violations. There are still 16 endpoints with hold violation.
Max utilization reached.
```

- Fix timing design rule violation
  - Max cap/Max slew/Max wirelength/Max fanout
- Fix hold time
- Fix setup time
- Cell sizing
- Buffer Insertion
- Load Insertion
- Buffer/load location

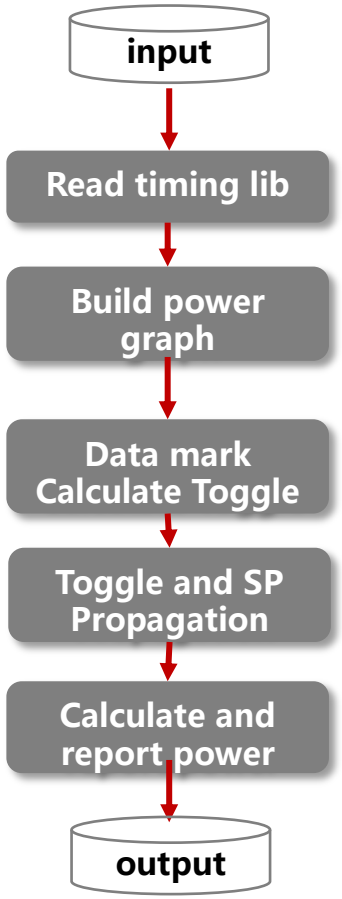
Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	-185.768	-1.27825
CLK_div2_core	-2606.7	-0.106129
CLK_div2_hs_peri	-216.759	-0.028571
CLK_div3_hs_peri	-72.5124	-0.028571
CLK_div4_core	-1304.1	-0.106129
CLK_div4_hs_peri	-185.768	-1.27825
CLK_div4_peri	-231.408	-0.042802
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	-89.8732	-0.028408
CLK_u0_clk_XC	-2987.42	-0.106129
CLK_u0_pll_FOUTPOSTDIV	-8546.64	-0.106129
CLK_u1_clk_XC	-2755.16	-0.106129

Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	0	0
CLK_div2_core	0	0
CLK_div2_hs_peri	0	0
CLK_div3_hs_peri	0	0
CLK_div4_core	0	0
CLK_div4_hs_peri	0	0
CLK_div4_peri	0	0
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	0	0
CLK_u0_clk_XC	0	0
CLK_u0_pll_FOUTPOSTDIV	0	0
CLK_u1_clk_XC	0	0

Hold report

Power Analysis (iPA)

Flow



API	Description
buildGraph	Build iPW graph data structure
readVCD	Parse the VCD file
buildSeqGraph	Build timing subgraph
checkPipelineLoop	Detect PipeLine loop
levelizeSeqGraph	Grade timing subgraph
propagateToggleSP	Propagate Toggle and SP data on the graph
calcLeakagePower	Calculate the leakage power
calcInternalPower	Calculate internal power
calcSwitchPower	Calculate switching power
analyzeGroupPower	Analyze power data
reportPower	Output power report

cases	iPA total power	Innovus total power	deviation
aes_cipher_top	22.22mW	23.74mW	6.4%
gcd	0.38mW	0.37mW	3.6%
uart	0.51mW	0.49mW	3.9%

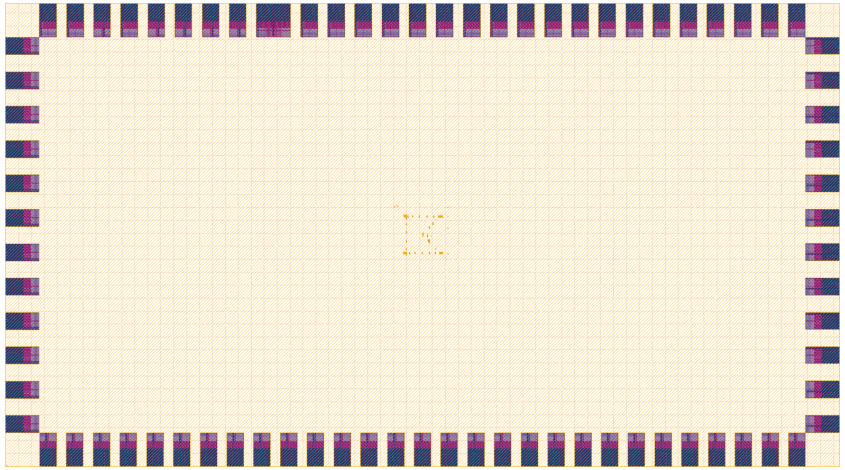
```
Generate the report at 2023-05-06T09:54:06
Report : Averaged Power
+--------------+---------------+-------------+--------------+------------+-----------+
| Power Group  | Internal Power | Switch Power | Leakage Power | Total Power | (%)       |
+--------------+---------------+-------------+--------------+------------+-----------+
| combinational | 1.064e-07     | 5.063e-09    | 3.079e-08    | 1.422e-07  | (27.595%) |
| sequential    | 2.862e-07     | 7.337e-09    | 7.963e-08    | 3.732e-07  | (72.405%) |
+--------------+---------------+-------------+--------------+------------+-----------+
Net Switch Power   ==    1.240e-08 (2.406%)
Cell Internal Power   ==    3.926e-07 (76.173%)
Cell Leakage Power   ==    1.104e-07 (21.422%)
Total Power   ==   5.154e-07
```

- Evaluate power before / during / after the physical design process
- Average model
- Timing window (coming soon)
- VCD parser
- Report/API

Conclusion

- **iEDA Objective**
  - **EDA Infrastructure**
  - **Explore new** and efficient **EDA method**
  - **High quality and performance EDA tool**

- **Open-source：(Gitee/Github)**
  - **GitHub: https://github.com/OSCC-Project/iEDA**
  - **Gitee: https://gitee.com/oscc-project/iEDA**



Open-source is not a goal but a way

- **Papers**
  - **iEDA:** An Open-source Intelligent Physical Implementation Toolkit and Library, ISEDA, 2023. (BPA)
  - **iPL-3D:** A Novel Bilevel Programming Model for Die-to-Die Placement, ICCAD, 2023.
  - **AiMap:** Learning to Improve Technology Mapping for ASICs via Delay Prediction, ICCD, 2023
  - **iEDA:** An Open-source infrastructure of EDA (invited), ASPDAC, 2024.
  - **iPD:** An Open-source intelligent Physical Design Tool Chain (invited), ASPDAC, 2024.
  - **AiEDA:** An Open-source AI-native EDA Library, ISEDA, 2024
  - **iRT:** Net Resource Allocation: A Desirable Initial Routing Step, DAC, 2024
  - **iCTS:** Toward Controllable Hierarchical Clock Tree Synthesis with Skew-Latency-Load Tree, DAC, 2024

OpenROAD

OpenLane

iEDA

CUHK EDA

OpenTimer

DREAMPlace

Thanks

Xingquan Li
lixq01@pcl.ac.cn