GPU Acceleration in OpenROAD: An Update

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GPU-Accelerated Global Placer: From DREAMPlace

DREAMPlace: <u>Deep Learning Toolkit-Enabled GPU Acceleration for</u> <u>Modern VLSI Placement</u>

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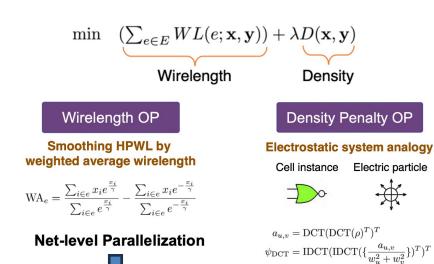
30X speedup

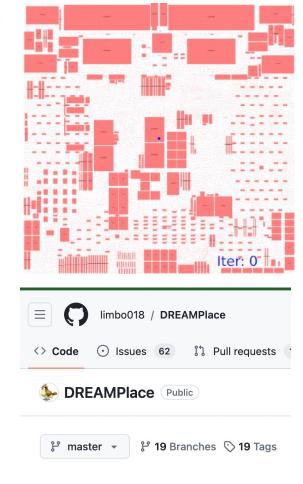
compared to RePIAce

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From DREAMPlace repo

Faster is great but not enough !

 $\xi_{\text{DSCT}}^{X} = \text{IDXST}(\text{IDCT}(\{\frac{a_{u,v}w_{u}}{w_{u}^{2} + w_{u}^{2}}\})^{T})^{T}$

 $\xi_{\text{DCST}}^{Y} = \text{IDCT}(\text{IDXST}(\{\frac{a_{u,v}w_{v}}{w_{v}^{2}}+w_{v}^{2}\})^{T})^{T}$

GPU-Accelerated FFT

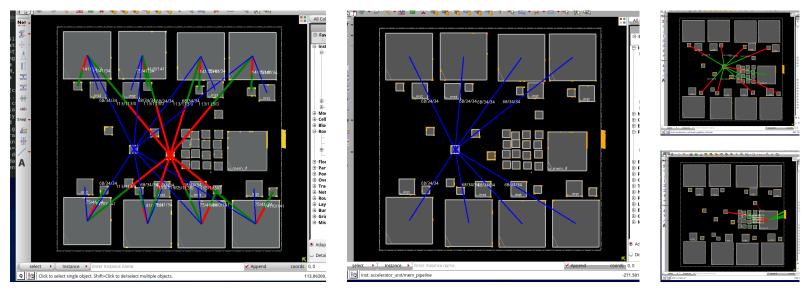
"Faster, Better, Cheaper – pick any two" (it's the law !)



Hints from Macro Placement

- Human experts usually need to consider multiple factors when they do macro placement
 - Dataflow
 - Connectivity between macros and input-output (IO) pins
 - Critical timing paths
 - · --

We also need to consider these factors when we do placement ! (Especially Mixed-Size Placement !!!)



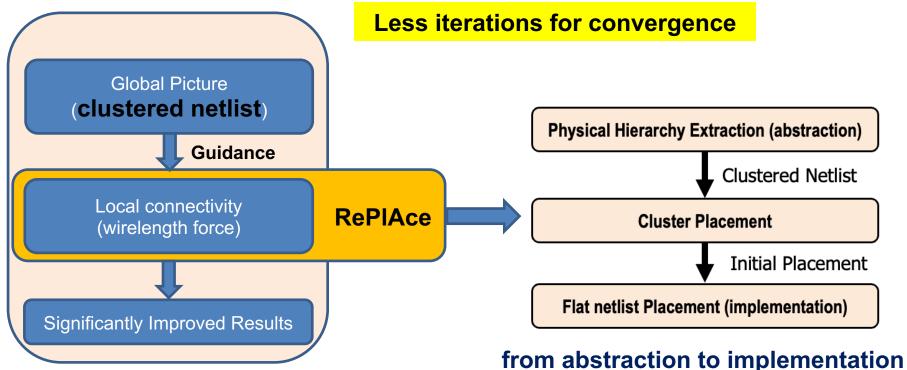


Example dataflow analysis of an AI accelerator

Clustering is another important lever !!!

Physical hierarchy aware placement

- Convert the logical hierarchy into physical hierarchy through merging and breaking logical modules (<u>TCAD'24</u>)
- Inform the placer about clusters of standard cells that will stay together during placement
 Better Placement
- Provide better initial locations for instances through cluster placement



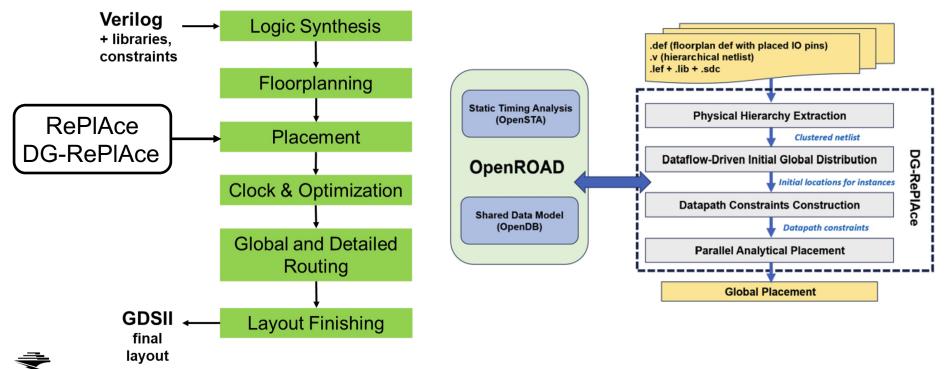
A. B. Kahng, R. Varadarajan and Z. Wang,

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"Hier-RTLMP: A Hierarchical Automatic Macro Placer for Large-scale Complex IP Blocks", IEEE Trans. On CAD, 2024.

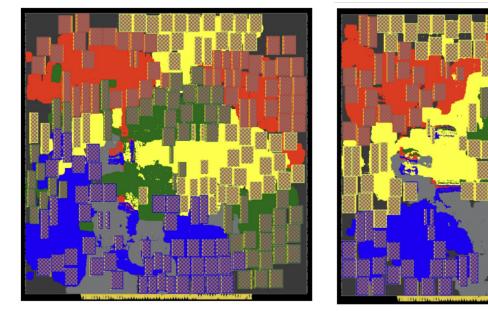
Dataflow-Driven GPU-Accelerated RePIAce

- Global Placer for large-scale IP blocks (DG-RePIAce) <u>arXiv</u>
 - Excellent Scalability: up to ~10M instances and ~1K macros
 - Superior Speed: more than 30X speedup compared to RePIAce
 - High Quality: dataflow-driven, physical hierarchy aware placement
 - Accessibility: fully open-source, integrated in OpenROAD src/gpl2
 - **Easy-to-use:** OpenROAD flow or plug into commercial productive flow



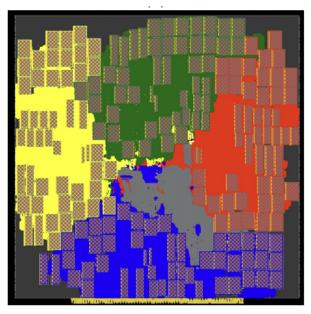
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Dataflow-Aware GPU-Accelerated RePIAce <u>arXiv</u>





DREAMPlace



DG-RePIAce

Global Placer	WL	Power	WNS	TNS	GP (s)	TAT (s)
RePIAce	1.00	1.00	-0.123	-108.15	387	653
DREAMPlace	0.92	0.98	-0.023	-2.623	61	88
DG-RePIAce	0.90	0.97	-0.014	-0.078	32	200

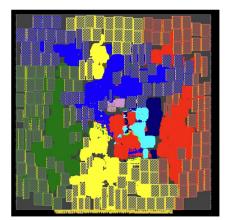
Testcase: BlackParrot RISC-V (Quad-Core) (evaluator: INVS 21.1) (827K stdcells, 196 macros in GF12LP)

Speed Enables Autotuning (NVIDIA AutoDMP)

Step 1: Specify hyperparameters

Hyperparameters (specified in configspace.json)

- coarsening_ratio: range = [6, 20], type = int
- max_num_level: range = [1, 2], type = int
- virtual_iter: range = [1, 8], type = int
- num_hops: range = [1, 8], type = int
- halo_width: range = [1.0, 3.0], type = float
- target_density: range = [0.5, 0.8], type = float





Demo: swerv_wrapper (NG45)

Post-route layout of RUN_ID = 14

A total of 29 uniqu		were sampled.							
A total of 29 runs were executed.									
The run took 10548.9 seconds to complete.									
<pre># Pareto-optimal points = 9</pre>									
rsmt	<pre> congestion </pre>	density							
:	:	:							
6 1.07373e+07	j 70.18 j	0.631724							
i 11 i 1.10367e+07	i 66.1 i	0.503092 İ							
14 1.09998e+07	69.44	0.508124							
17 1.08384e+07	70.97	0.554149							
18 1.07772e+07	68.33	0.581476							
22 1.08833e+07	69.77 i	0.558474							
25 1.08008e+07	i 64.91 i	0.563338							
26 1.07329e+07	68.42	0.68759							
27 1.08633e+07	j 77.63 j	0.550306							
Pareto candidates:									
rsmt	<pre> congestion </pre>	density							
:	:	:							
14 1.09998e+07	69.44	0.508124							
17 1.08384e+07	i 70.97 i	0.554149 İ							
18 1.07772e+07	68.33 i	0.581476							
26 1.07329e+07	68.42	0.68759							
27 1.08633e+07	77.63	0.550306							

	RUN_ID	WL	Power	WNS	TNS
-	default	0.90	0.972	-0.014	-0.078
	14	0.86	0.967	-0.002	-0.007
	17	0.85	0.971	-0.014	-1.048
	18	0.86	0.968	-0.012	-0.216
	26	0.85	0.969	-0.027	-1.794
	27	0.86	0.970	-0.007	-0.139

Step 3: Run INVS P&R for Pareto candidates

Step 2: MOTPE Bayesian Opt tuner

GPU-Accelerated Router [Ongoing]

Router plays a central role in the physical design flow

- A chip will never be taped out if the router cannot achieve DRC-clean routing solutions.
- Routing is the most timing-consuming step in the physical design flow.
- GPU-accelerated router is still pending today. [Kahng24ISPD]
- TritonRoute-WXL (2021) is the state-of-the-art academic detail-routabilitydriven unified global-detailed router. <u>paper</u> <u>src/drt</u>
- A new GPU-accelerated global router for TritonRoute-WXL is on the way !

• Our goals:

- Excellent scalability and superior speed: handle designs with 50M nets in half an hour
- **High quality**: achieve better performance as TritonRoute-WXL
- Fully open-source: integrated into OpenROAD
- Easy-to-use: used as real global router in the physical design flow or used as academic eGR for early evaluation (replace RUDY in AutoDMP)



We want a better open-source GPU-accelerated EDA ecosystem !

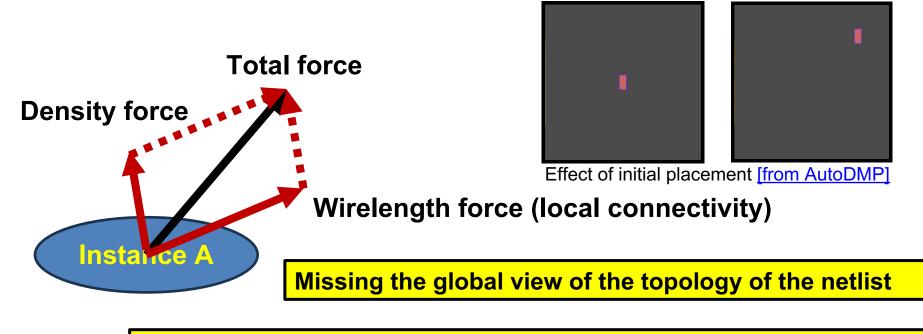
THANK YOU !



Clustering is another important lever !!!

Clustering → better and faster placement (Get Both!)

- Better placement: telling the placer how a near-optimal placement looks like
- Faster placement: providing a better initial placement, thereby reducing the number of iterations needed for convergence



Instances that should stay together may be far away from each other

Solution: tell the placer which instances have more chance to stay together

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