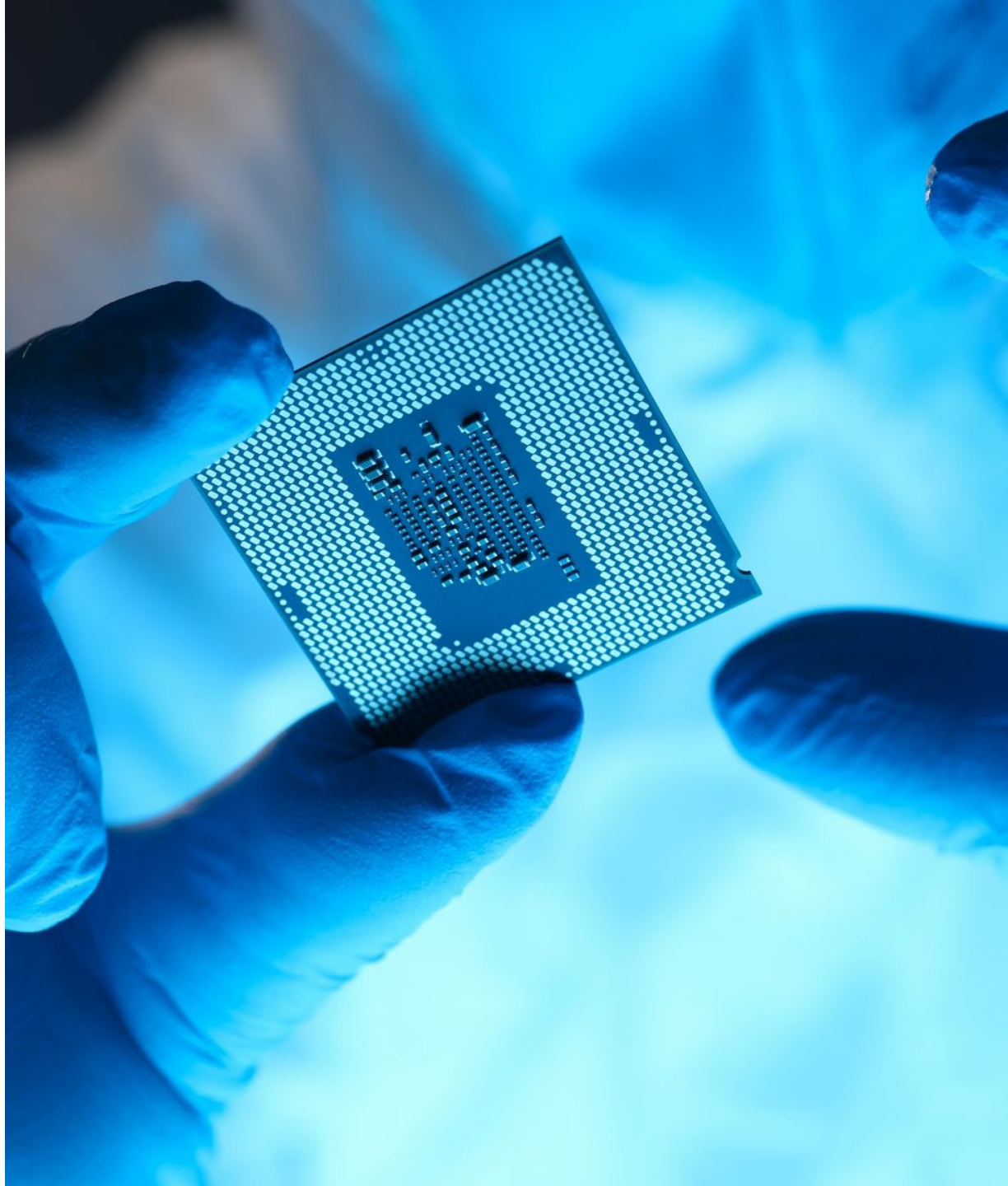
ChipFlow

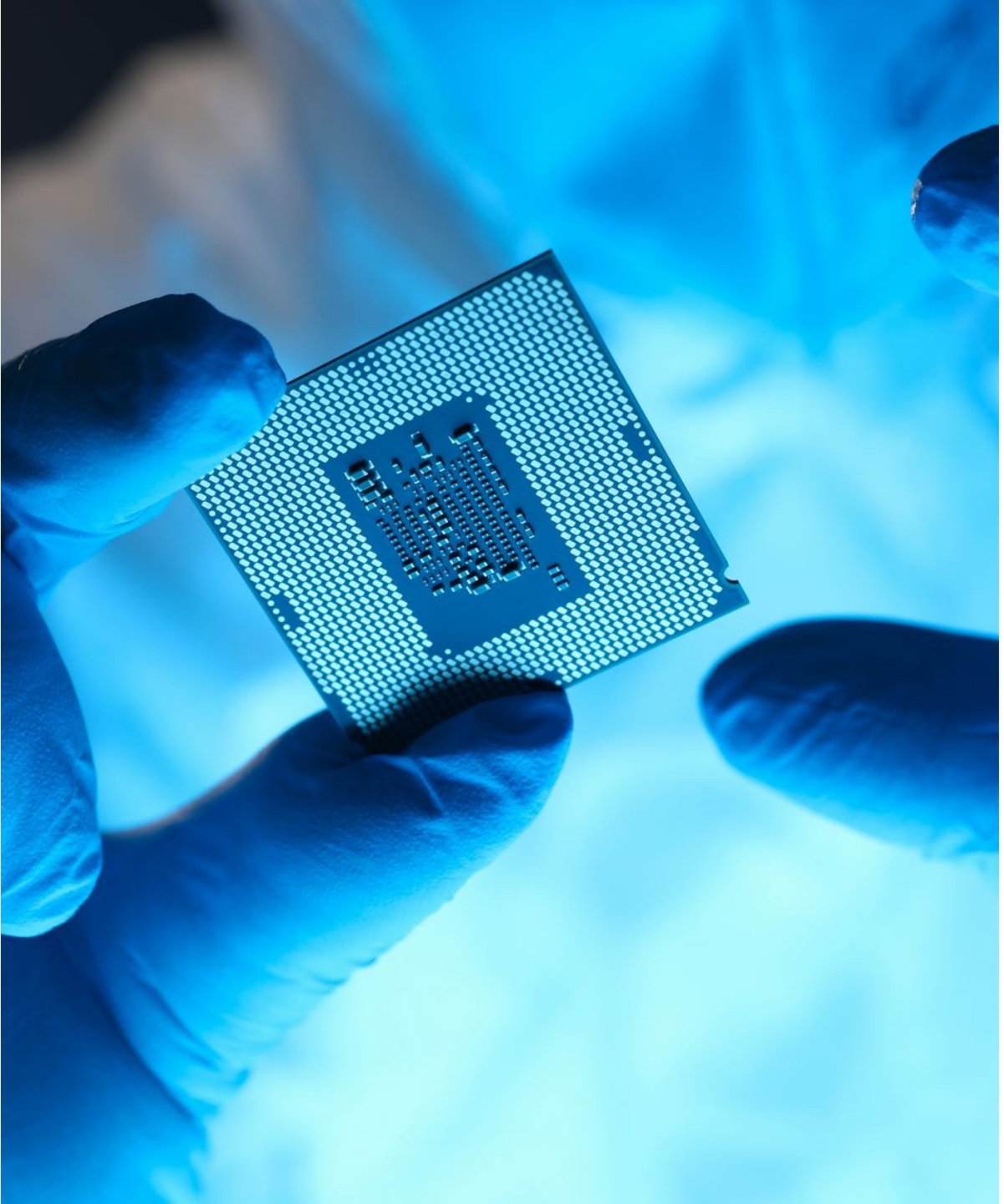
Introduction and Progress Update

DAC
June 25th 2024



A Brief History

- Started in 2021
- Registered in the UK
- Team members located in UK, France, Germany, Belgium, US
- Pre-seed round in 2023 (Fontinalis, InMotion, others)
- Currently closing Seed round
- Currently executing **proof of concept designs** with partners



ChipFlow in a Nutshell

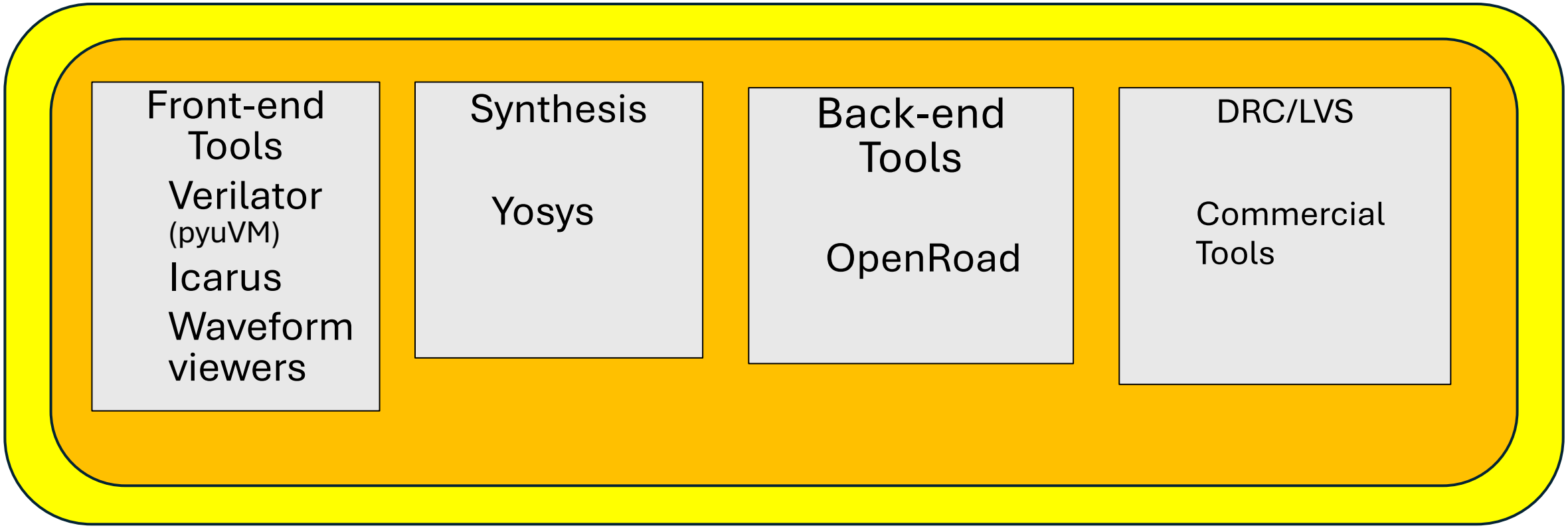
ChipFlow's goal is to provide an open-source based platform for low-cost development of custom ASICs

Front-end (RTL) design is done by customer, along with front-end verification based on open-source EDA tools using ChipFlow's platform in the cloud

Back-end design and sign-off are handled by ChipFlow using open-source EDA tools, in maximally automated manner, and invisible to the customer

Foundry and OSAT interface (supply chain) are managed by ChipFlow

The ChipFlow Platform during the Proof of Concept Phase

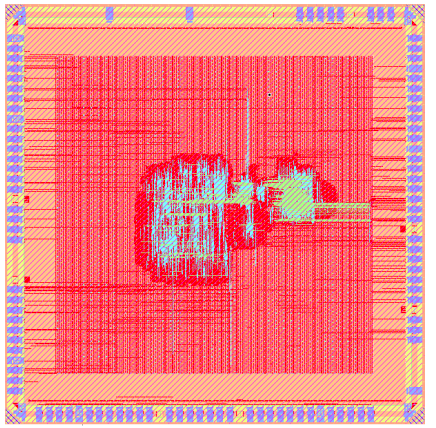


- All front-end design and verification done by ChipFlow working with customers' specifications
- ChipFlow progressively automates the Synthesis to GDSii flow
- Post-tapeout work with foundry, OSAT partners managed by ChipFlow

Proof of Concept Design Example

A large automotive OEM needs a path forward for overhauling their **electronic architecture.**

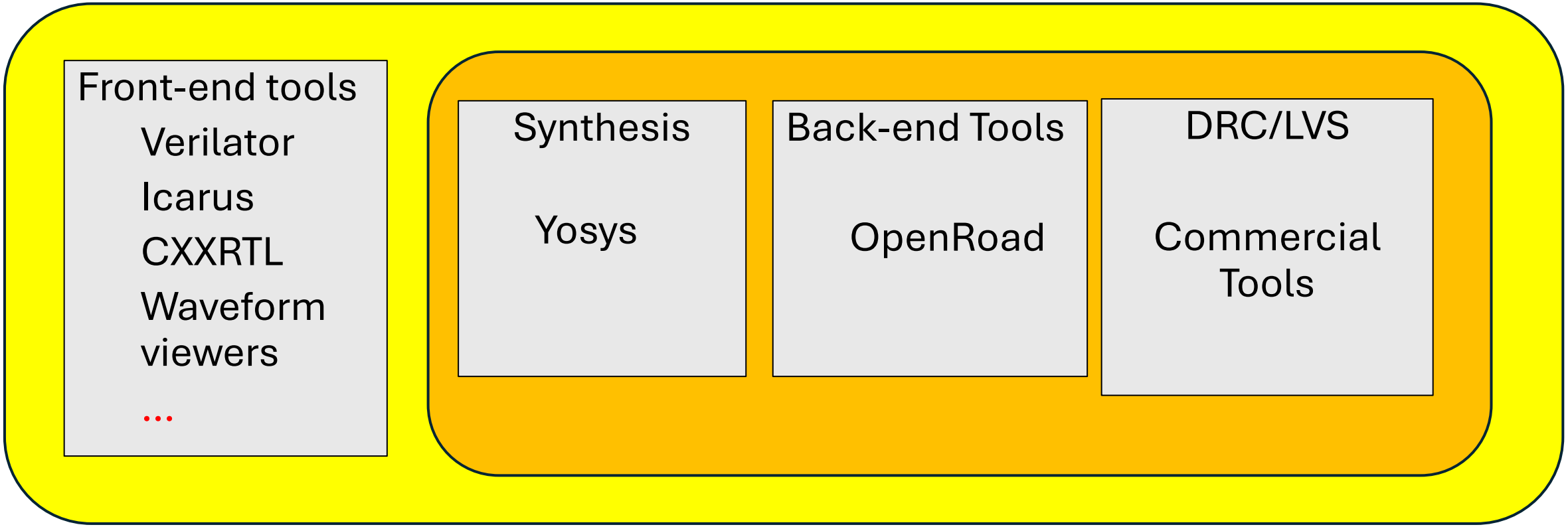
The **ChipFlow platform** was used by ChipFlow engineers to deliver an all-in-one custom ASIC against their requirements for **full door functionality.**



Initial test chip was designed in **3 months**, and taped out using GF 130nm process technology (through Fraunhofer, on MPW)

This custom solution potentially can replace ~ **10 ICs** with **1 IC,** allowing a major savings on the budget for harness and electronics.

The ChipFlow Platform in Production



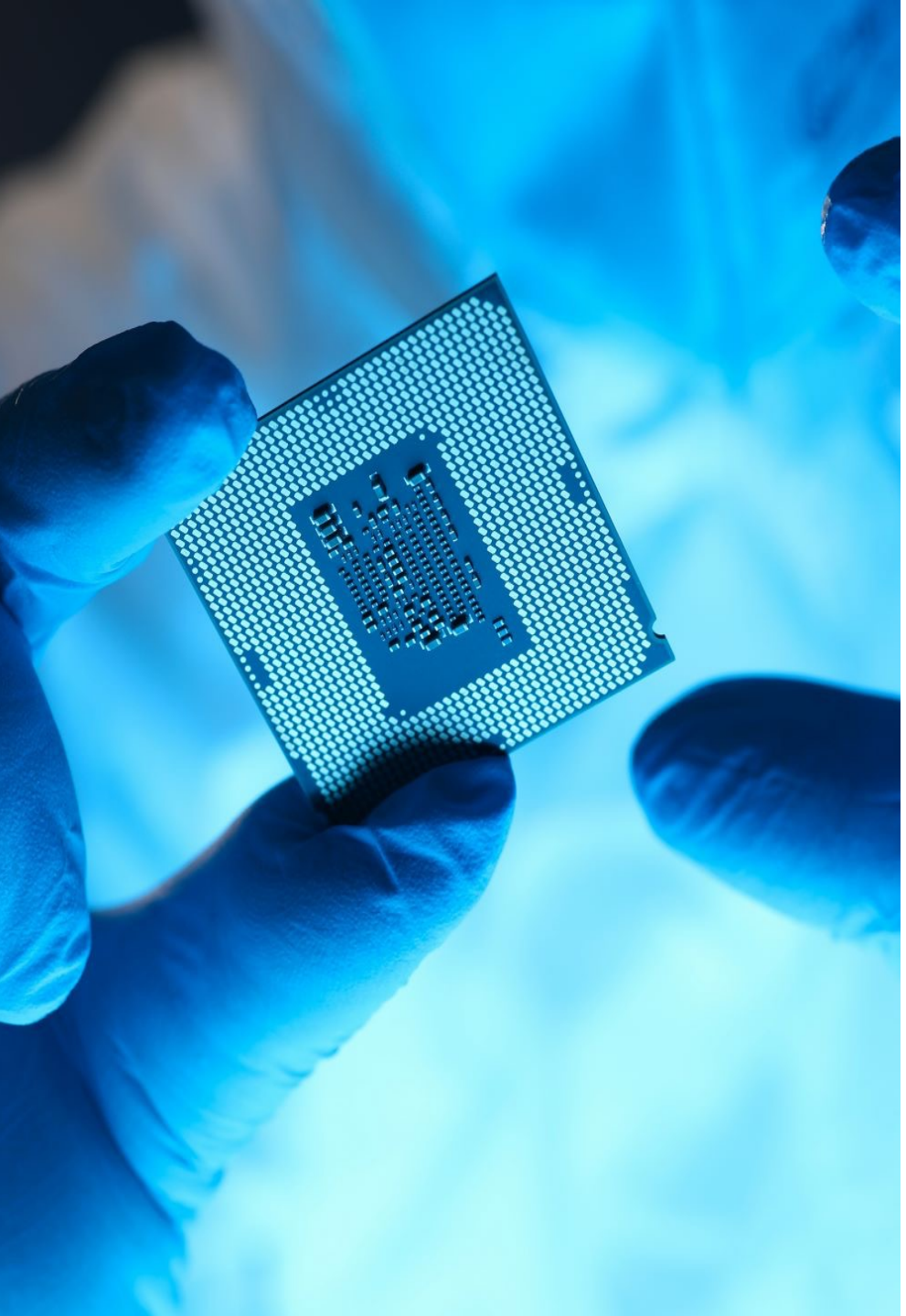
- Customer only interacts with front-end tools
- ChipFlow automates the Synthesis to GDSii flow
- Post-tapeout work with foundry, OSAT partners managed by ChipFlow

ChipFlow Contributions to Open-source EDA

- ChipFlow funds, and its engineers are active developers in, several open-source EDA projects :
  - PDKMaster, a tool for automated standard cell library generation
  - Amaranth, a Python-based hardware design language
  - CXXRTL, a fast RTL level simulator

Experience with Open-source EDA tools

- Many areas of EDA are well covered by open-source tools
  - RTL Simulation
  - Place and Route
  - Static Timing
- We perceive some gaps in the overall open-source EDA tools landscape, e.g. :
  - Mixed-Signal Verification
  - Logical Equivalency Checking
- We are interested in collaborating on projects in these and other areas



Upcoming ChipFlow Events

Training on Chip Design using Open Source EDA tools
@ imec, Louvain, Belgium

November 25th-26th 2024

Contact

https://www.chipflow.io/