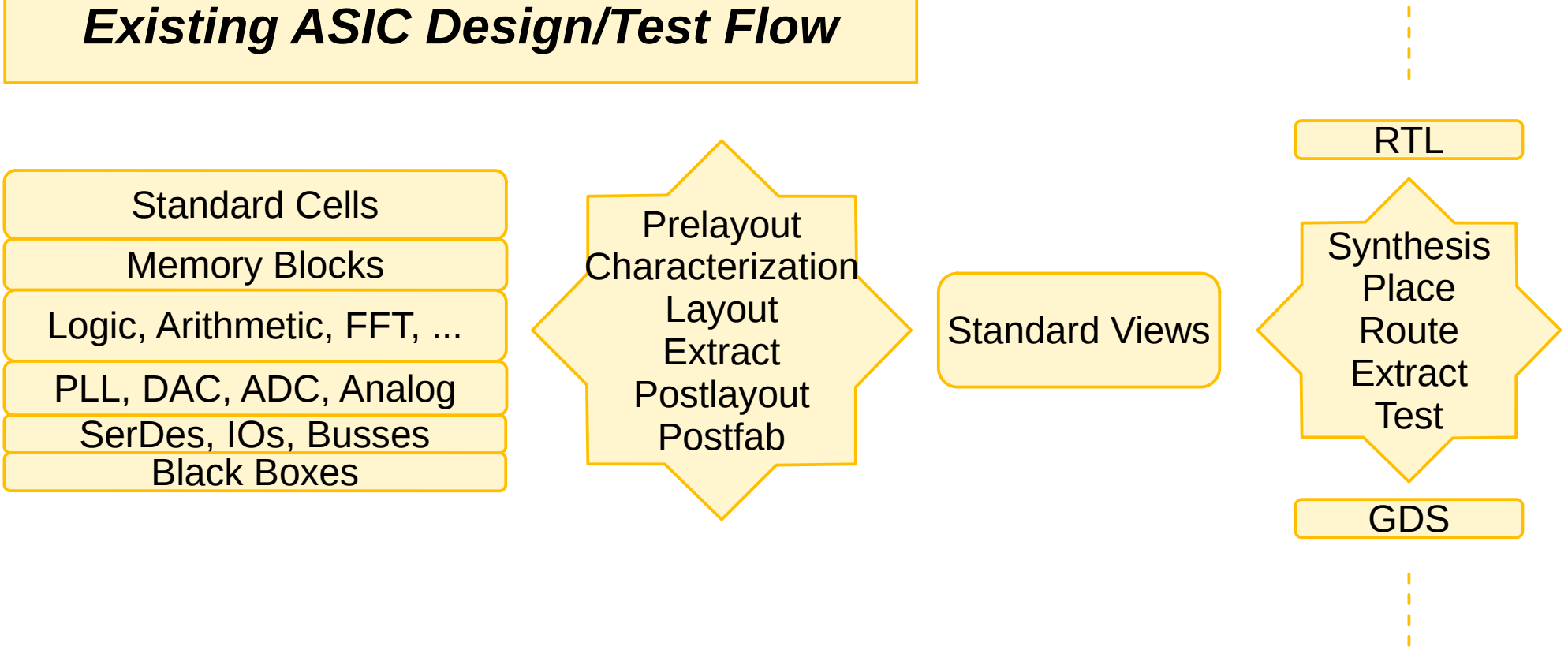
Existing ASIC Design/Test Flow



Agnostic HDL & Compiler

HDL

Compiler

- **Standard Cells**
- **Memory Cells**
- **Logic, Arithmetic**, FFT, ...
- PLL, DAC, ADC, **Analog**
- SerDes, IOs, Busses
- **Black Boxes**

Prelayout
Characterization
Layout
Extract
Postlayout
Postfab

Standard Views
Liberty

- Digital/Analog
- Sync/Async

- Sized Transistor SPICE Netlist
- Characterization/Test Bench

6 months x 1 man

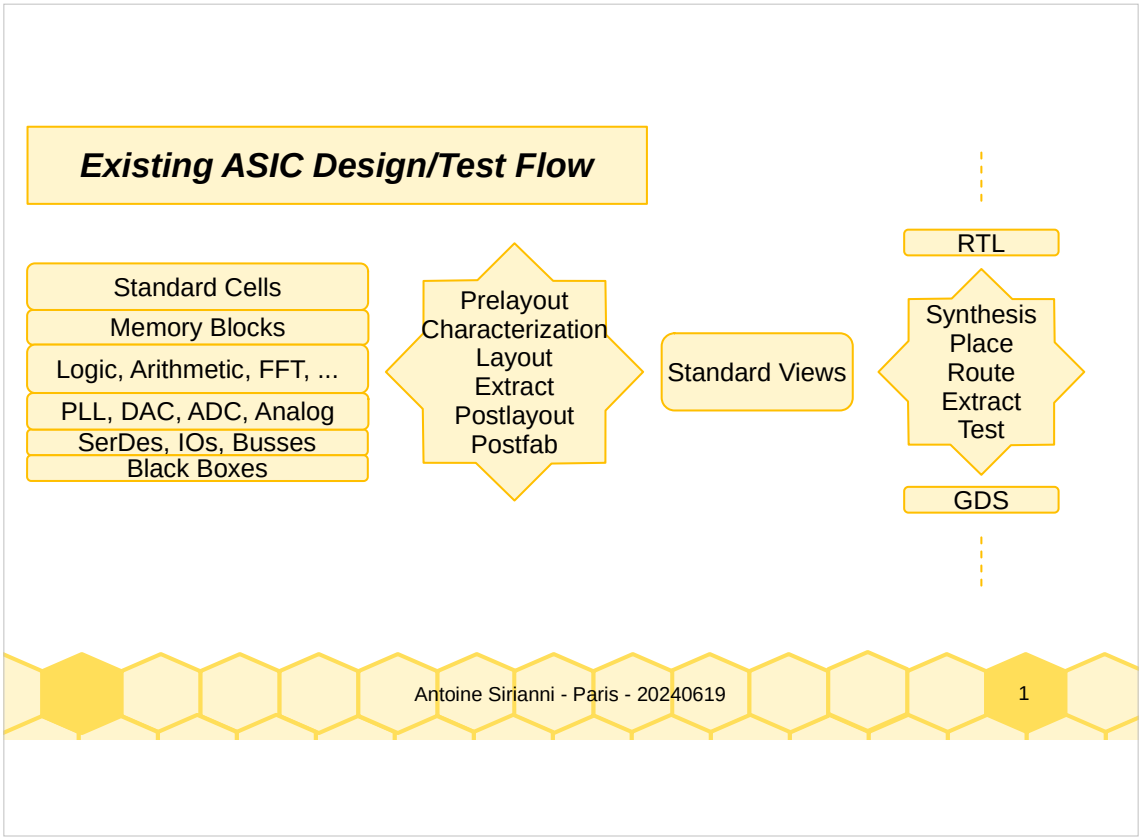
COOPER: Hey, TARS, what's your honesty parameter?
TARS: Ninety percent.
COOPER: Ninety percent?
TARS: Absolute honesty isn't always the most diplomatic, nor the safest form of communication with emotional beings.

Interstellar

- Intel i5 20 cores 80 GB / Nvidia 4070 Ti GPU 12 GB
- Linux Ubuntu 22.04.1
- gedit, typora, libreoffice, ...
- flex, bison, gcc, python, make, git, ...
- xschem, ngspice, ...
- FreePDK45, ...
- **ChatGPT : Amazingly helpful :-)**

Fine tuning LLMs with std views?
Are LLMs the next platforms?

contact: antoine.sirianni@free.fr



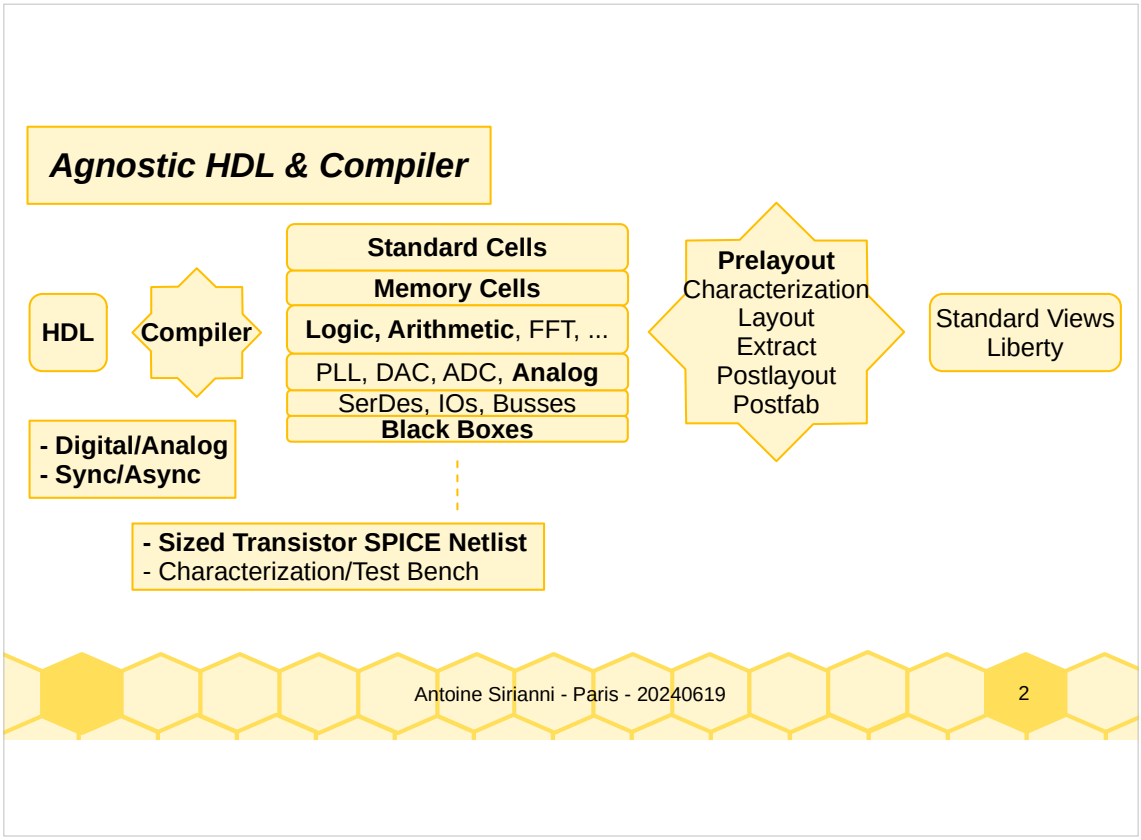
Hello,

My name is Antoine Sirianni. I am a seasonned EE/CS Engineer/PhD with a specilization in microelectronics.

I have just participated to the FSiF 2024 events in Paris where I had the honor to meet with Pr. Andrew B. Kahng.
I would like to express my warmest thanks to him to kindly welcome this presentation to DAC BOF 2024.

As you know, any RTL to GDS flow requires libraries of components to operate.

These components are generally part of the targeted technology PDK. They may also come as 3rd party IP blocks or may be designed in-house.

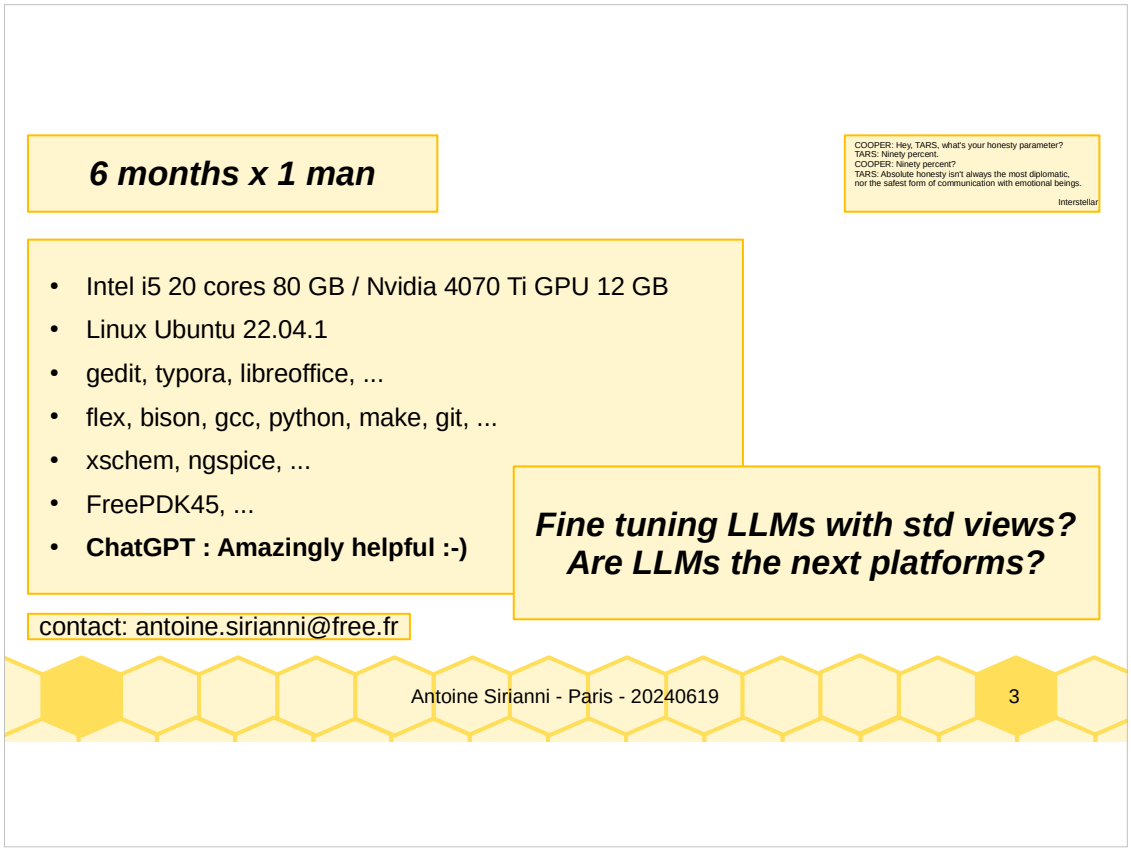


What if some compiler would be able to produce libray components from some code written using an agnostic HDL ?

By agnostic I mean :
- supporting digital, mixed or analog designs,
- supporting synchronous or asynchronous designs.

For instance, to start with, such a compiler would produce sized transistor SPICE netlists that could be used to feed a standard cell characterization flow.

The bold words show you where this project is standing to date.



What would be the impact of this project ?
- Increase the level of automation of library design
- Ease library optimization
- Ease library qualification
- Ease architecture exploration
- Enable LLMs fine tuning with qualified library data
- What do you think ?

What part of this project would you like to see become open source ?

Would you be ready to support it ?

Thank you for your attention !
Thank you for your feedback !