From Walking to Running

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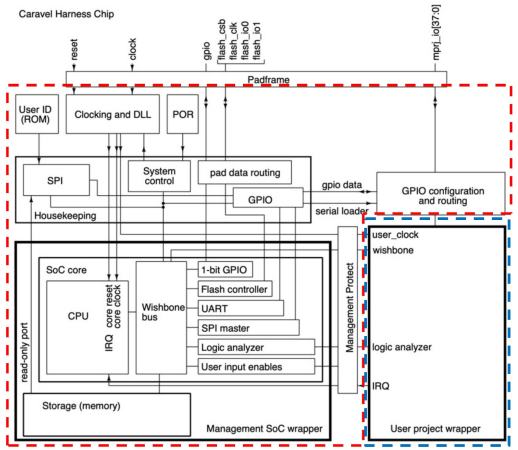
SVP R&D and New Product Introduction

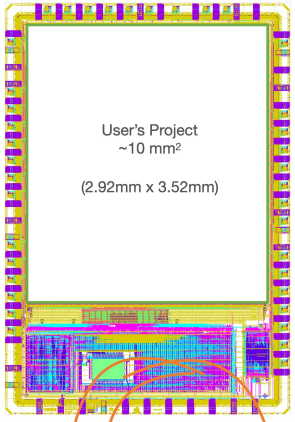
efabless.com

Birds of a Feather DAC 2024

Caravel Open Source SoC Platform

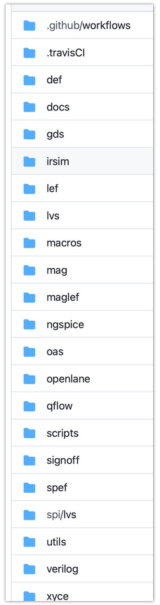


https://github.com/efabless/caravel



VexRISCV OpenRAM
OpenROAD OpenLane

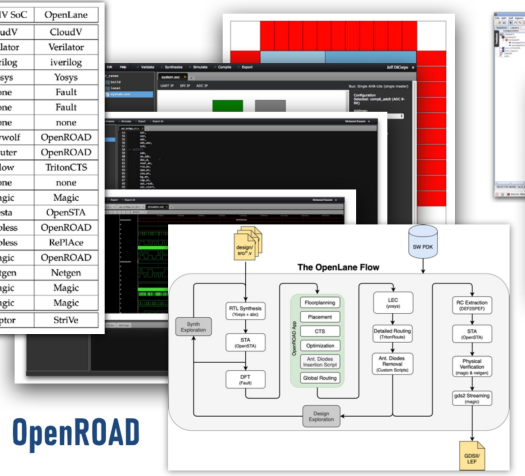
Uniform Open Source File Structure to ease reuse & modifications



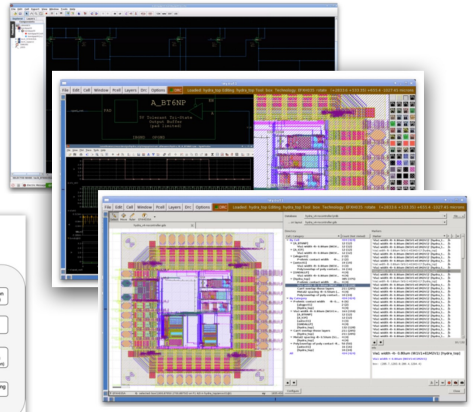
OPEN SOURCE DESIGN FLOWS, PDK & IP

DESIGN STEP	Qflow	CloudV SoC	OpenLane
System Design	N/A	CloudV	CloudV
RTL Lint	Verilator	Verilator	Verilator
RTL Simulation	iverilog	iverilog	iverilog
Logic Synthesis	Yosys	Yosys	Yosys
DFT Scan Insertion	none	none	Fault
DFT ATPG	none	none	Fault
Formal Verification	none	none	none
Placement	graywolf	graywolf	OpenROAD
Routing	qrouter	qrouter	OpenROAD
CTS	Qflow	Qflow	TritonCTS
Dynamic EMIR	none	none	none
Extraction	Magic	Magic	Magic
Timing Analysis	Vesta	Vesta	OpenSTA
Floorplanning	Magic	efabless	OpenROAD
Top-Level Placement	Magic	efabless	RePlAce
Top-Level Routing	Magic	Magic	OpenROAD
LVS	Netgen	Netgen	Netgen
DRC	Magic	Magic	Magic
GDS	Magic	Magic	Magic
SoC	Raven	Raptor	StriVe

- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

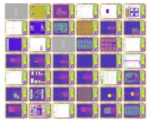


OpenROAD



OpenLane

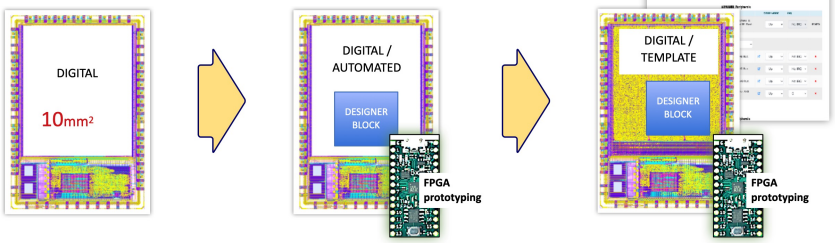
- Schematic Capture
- SPICE Simulation
- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification



One Size Fits All

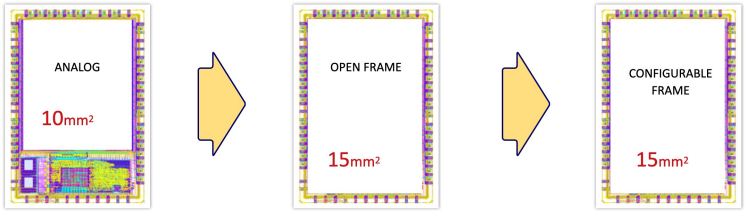
LOW COMPLEXITY

IP Development
Digital & low frequency analog
Enabling larger designer base



HIGH COMPLEXITY

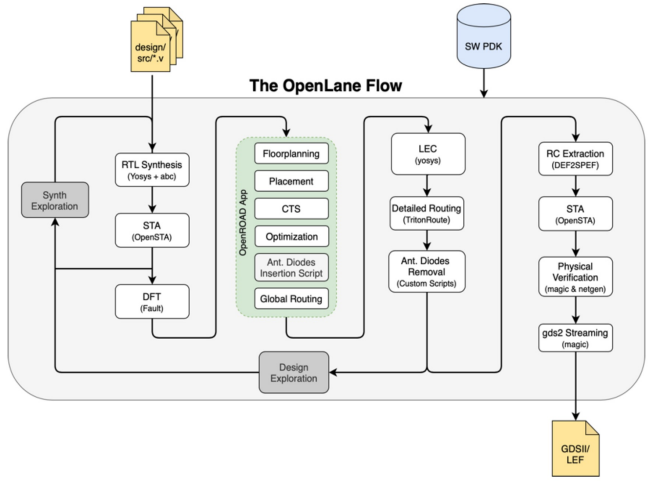
IP Development
Complete Custom ASIC
Analog & Digital
Expert designer base



OpenLane DIGITAL COMPILER-LIKE RTL2GDS

Automate code-to-chip like a ***GNU software compiler*** - *with trade-offs in area and performance.*

It opens the door for software developers to generate hardware
That's at least a 100x more potential designers!



Shuttle Schedule

	CI 2404	CI 2406	CI 2409	CI 2411
Engineer Samples	100 QFN	100 QFN	100 QFN	100 QFN
Evaluation Boards	✓	✓	✓	✓
Submission Deadline	Apr 24, 2024	Jun 3, 2024	Sep 16, 2024	Nov 11, 2024
Delivery*	Sep 2024	Nov 2024	Feb 2025	Apr 2025
Bare Die Option	✓	✓	✓	✓
Reram Support	✓		✓	

Production Volume

chipIgnite provides an easy path from prototyping to low, medium and high volume production. The solution allows customers to share masks and fabrication costs with others, making low volume production more affordable.

	Prototype Volume	Production Eval	Low Volume	Medium Volume	High Volume
Number of Parts	**100**	**1000**	**10,000**	**100,000**	**1,000,000 +**
Maskset	Shared	Shared	Shared	Shared	Dedicated
# Wafers	< 12	12	50 - 100	200 - 400	1000+
Packaging	64L QFN, Bare Die	64L QFN, Bare Die	8, 16, 32, 64L QFN/SOIC, Bare Die	8, 16, 32, 64L QFN/SOIC, Bare Die	Fully custom
Production Test	--	--	✓	✓	✓

IP Marketplace

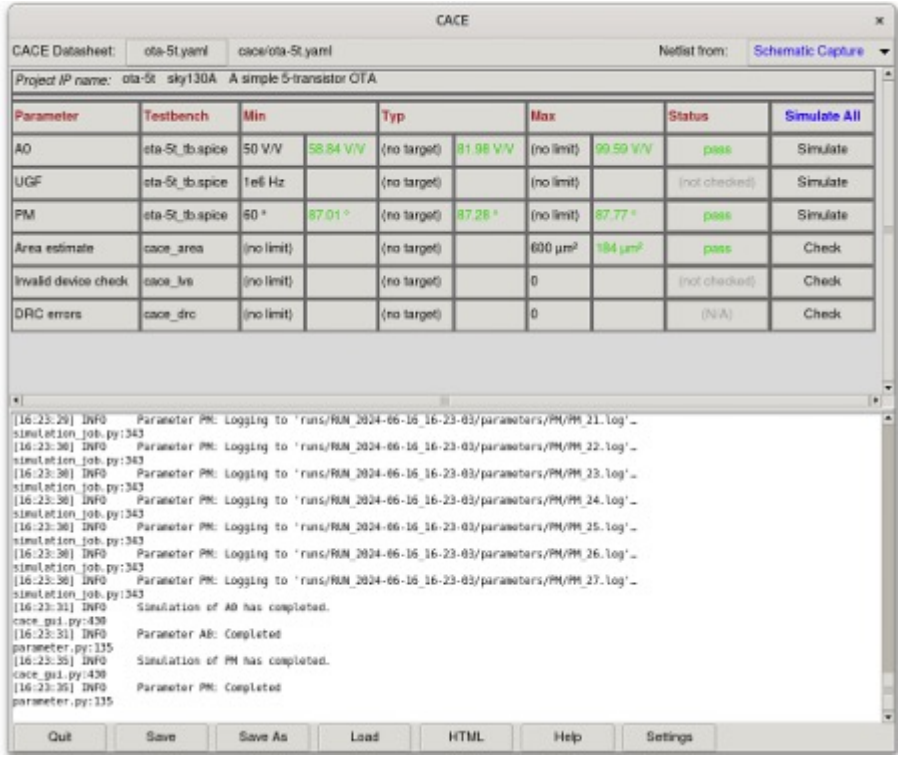
Efabless marketplace is a one stop shop for digital, analog and analog mixed signal IPs, developed by Efabless and the community.

Available IPs on the Marketplace		
Digital	Analog	
4KByte Commercial SRAM	Ultra low-power comparator	HGBW Operational amplifier
16KByte Commercial SRAM	Instrumentation amplifier	Over-voltage detector
32KByte Commercial SRAM	LP Operational amplifier	Brown-out detector
GPIO peripheral	Comparator	Temperature sensor
32-bit timer and PWM generator	1.8v Precision bandgap	Low-speed XO
Quad SPI Flash memory controller	Low-power 1.8v LDO	High-speed XO
DFFRAM512x32	Current reference bias generator	Programmable PLL
DFFRAM256x32	16-bit capacitive DAC	Programmable Sallen-Key filter
DFFRAM128x32	12-bit resistive DAC	Bandgap-referenced Power-on-Reset
UART	8-bit Rheostat	16-bit SAR ADC 1MSPS
I2S receiver	12-bit IDAC	
I2C master controller		
SPI master controller		

Getting started with Cace

Automate anything that you will do more than twice

- Circuit Automatic Characterization Engine
- Using CACE saved time
- CACE increased probability of success
- CACE is actively supported
- CACE is both FREE and Open
- CACE supports CI
- https://github.com/efabless/cace



Productivity Impact

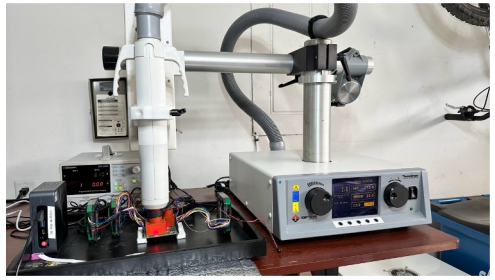
- Reduced HC design teams
- Short time from Concept to Cash
- Reduced Complexity
- Lower Cost

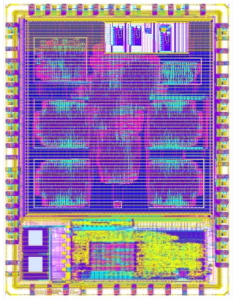
6 designers, 91 weeks, 11Chips

<$110K Silicon Cost

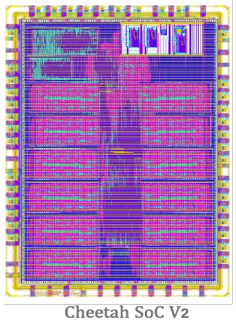
<$20K Capital Cost

Full Temp and Voltage “Char”

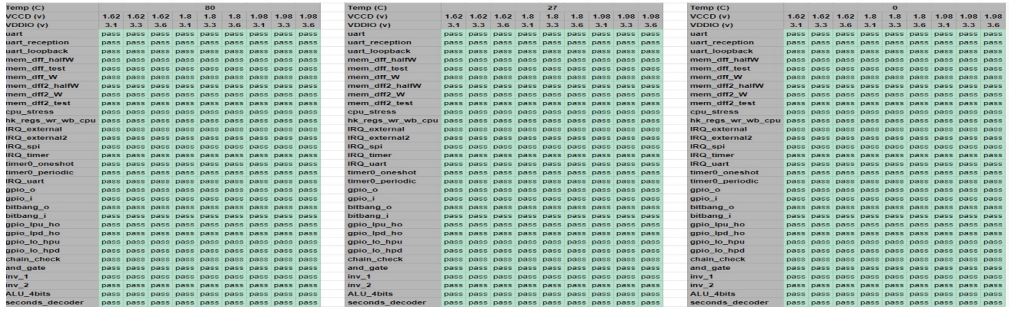




Cheetah SoC V1
Taped out: Sept. 23
Caravel



Cheetah SoC V2
Taped out: Nov. 23
Open Frame



Fixed Caravel 1
1st Taped out: Dec. 22
Based on Caravel

Caravan
Taped out: Apr. 23
Based on Caravel

Cheetah 2
Taped out: Nov. 23
Based on Open Frame

Blizzard
Taped out: Apr. 23
Based on Caravel

Cheetah 1
Taped out: Sept 23
Based on Caravel

Caravel V2
Taped out: Nov. 23
Based on Open Frame

Swift
Taped out: Apr. 23
Based on Caravel

OpenFrame
Taped out: Jun. 23
Based on Caravel

Clear
Taped out: Apr. 23
Based on Caravel

Caravel DFT
Taped out: April. 24
Based on Open Frame

Cheetah 3
Tape out Planned : Jul. 24
Based on Caravel V2

Running with Analog:

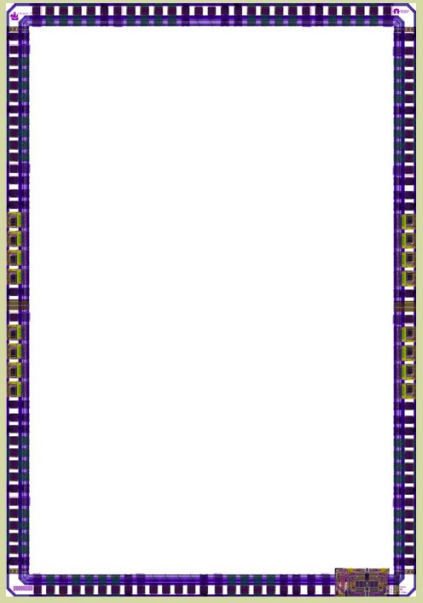
38-64 GPIO, 0-16 OVT IO,

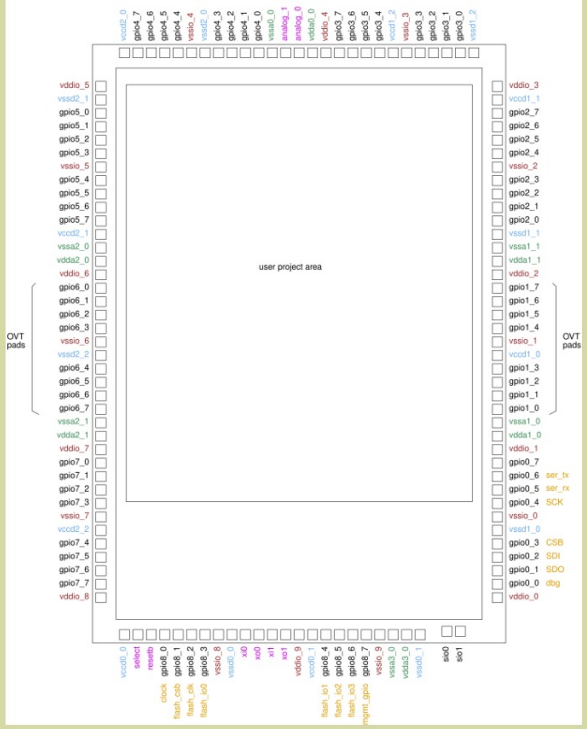
SIO with analog for differential IO.

4x the power for the IO ring SSO.

Full 50Mbits/s throughput.

Analog mux IO useable

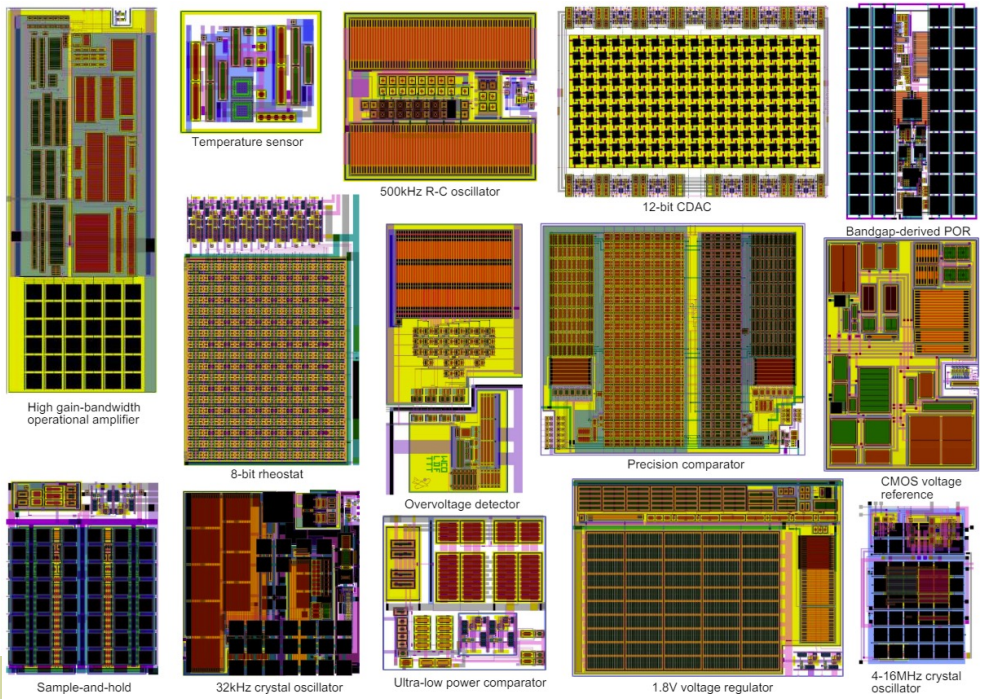




64 user/mgmt GPIO
- 8 mgmt GPIO
- 2 SIO pads
- 2 analog pads

16 GPIO are OVT
- 4 XO pads

8 1.8V supply pins
8 1.8V ground pins
9 3.3V supply pins
9 3.3V ground pins
6 analog 3.3V pins
6 analog ground pins



Running with IO and Analog

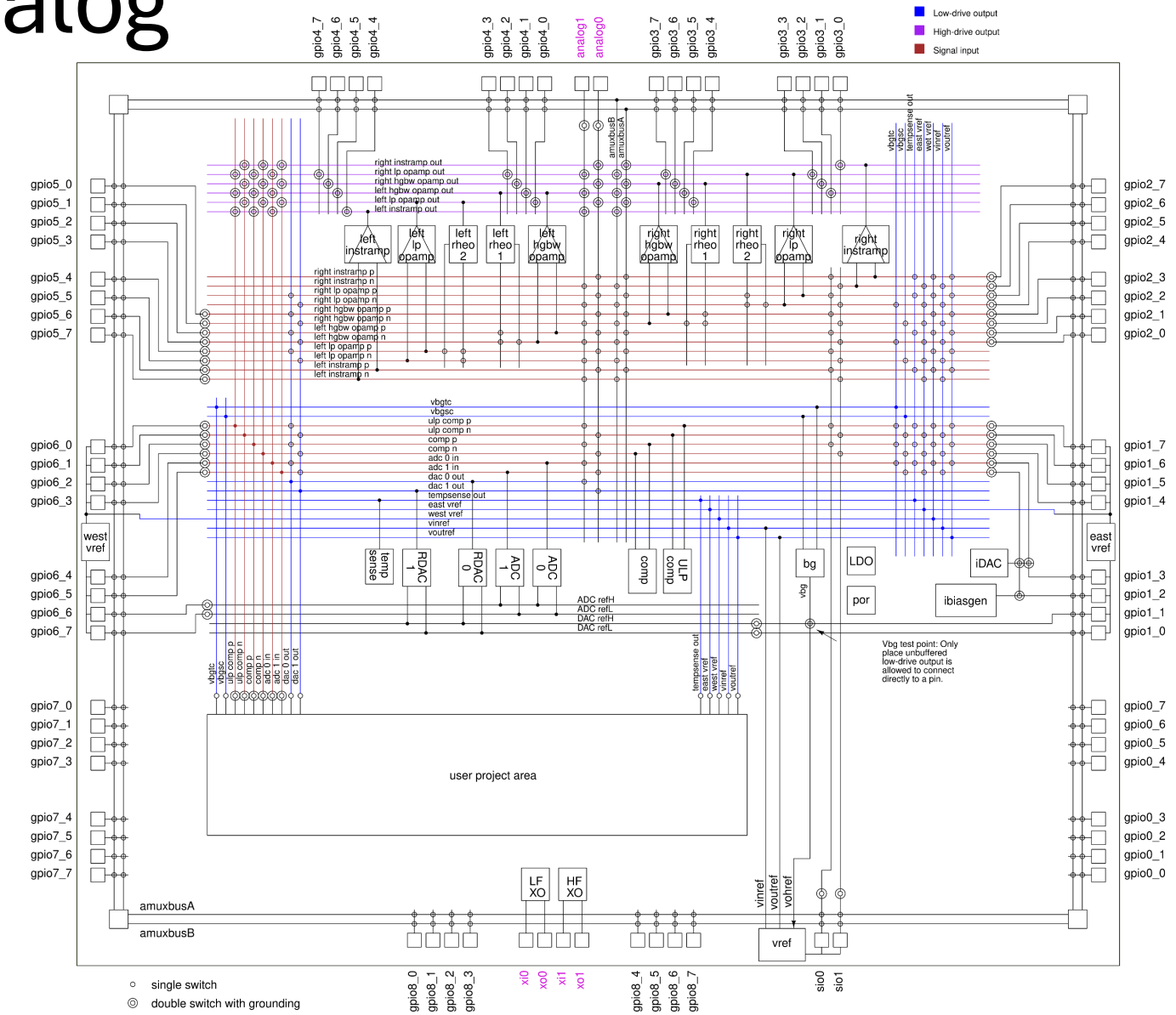
20X the included analog IP

~30x the available analog IP

2 oscillators

2 crystal connections

Analog SOC architecture



NOTES:

1. The biasing network is not depicted. ibiasgen takes input from the bandgap and distributes currents to all blocks requiring them.
2. All names should match the names used in the verilog, schematic, and layout of the cheetah_v3_analog block and subcircuits.
3. There are direct connections from pads on gpio3 and gpio4 (16 total) to the user project area that are not depicted.
4. There are two outputs from ibiasgen (50nA and 100nA) routed to the user project area that are not depicted.
5. The switches shown between each GPIO and SIO pad and amuxbusA and amuxbusB are part of the pad cell, not the analog subsystem.

Getting started with Digital IP

OS Digital and Systems IP:

- 5X the available digital peripherals
- 4X higher Flash IF bandwidth
- >100X higher CPU throughput with Cache optimiztion
- Embedded accelerators included
- Coming Soon: 2D convolution and CNN accelerator

Commercial:

- Commercial SRAM in Q2 24
- Commercial OTP prototype tapeout in Q3,
- Commercial Flash in Q4
- Coming Soon: Custom ML model flow and ML accelerators.

Other Templates:

- Caravel/4

Beginning to Fly:

How can the community help:

Our immediate needs to increase traction and fund continueing operations:

Efficient compute parallelism on all job types (Sims, Verification, Extraction, DRC).
We are floating the compute and as designs get more complex it is getting expensive. We need both efficiency and parallelism.)

Flow: UVM enhancements, UPF completion, Clock tree enhancements, IR Drop, Advanced DFT

Analog IP: Standardized Repo structure adoption. 16b 1MSPS ADC, Advanced 2^{nd} and 3^{rd} order programmable Filter Functions.

Digital IP: Advanced motor control, 32bit MCU peripherals , Programmable DSP block, Improved eFPGA, Accelerators.

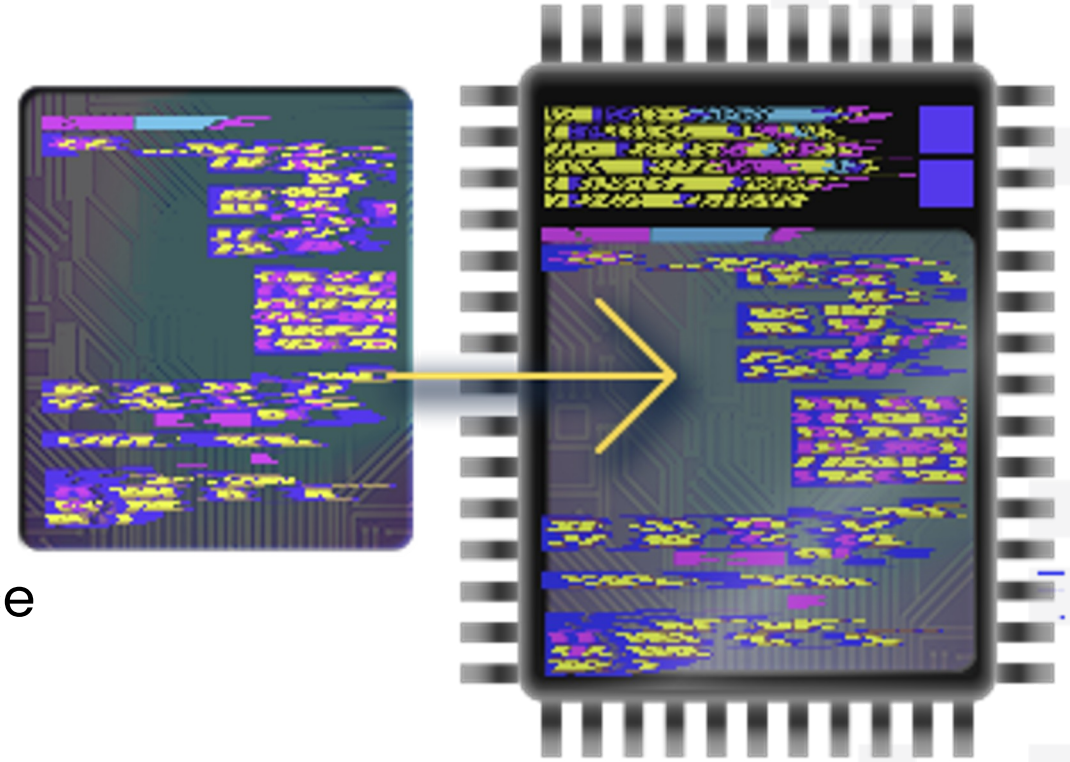
Memories: RAM and DP RAM macros.

EcoSystem: Security Solution, Cloud Stack, Radio SIP suggestions

IDE standardization: Getting users to the benchmark flows quickly with all the tools for Analog, MS and OL/OR.

chipignite Empowering Innovation in IC Design

- Innovative Design Platform
- Cost-Effective Solution
- Rapid Development Cycle
- Flexible and User-Defined
- Robust Community Support
- Enhanced Supply Chain Resilience



Running with: chipignite

Thank You to the entire OS Community!

This could not be built without your contributions

We need your input:

What do you need to succeed?

Video Tutorials - https://efabless.com/getting-started

Join Our Slack Community - https://open-source-silicon.dev/

Contct Us – shuttle@efabless.com

Visit Us – www.efabless.com