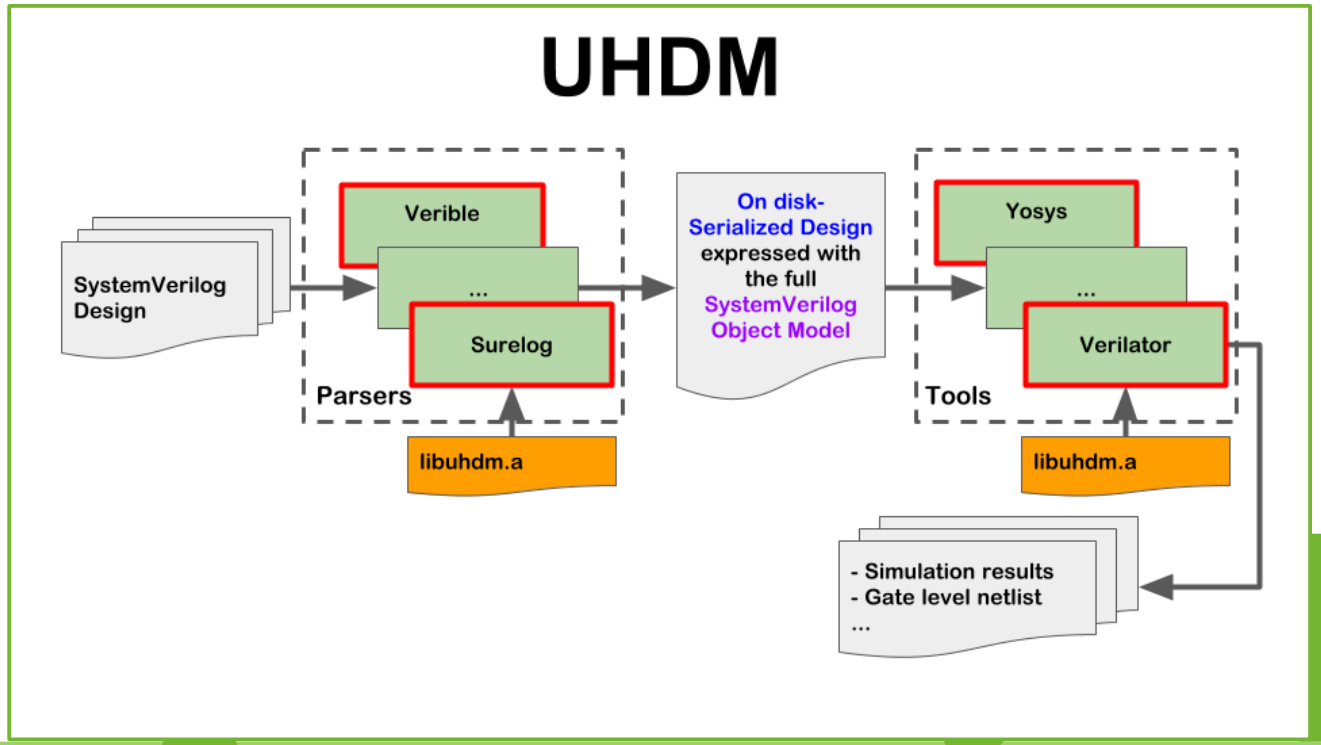
Surelog/UHDM : Open-source SystemVerilog Compiler

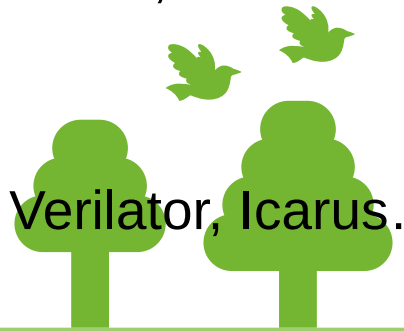


- Hosted by ChipsAlliance:

  https://github.com/chipsalliance/Surelog **SV2017 Preproc, Parser, Compiler, Elaborator, UHDM writer**

  https://github.com/chipsalliance/UHDM **Universal Hardware Data Model**

  chipsalliance/yosys-f4pga-plugins/tree/main/systemverilog-plugin **Yosys SV-plugin**
- Started 2017, sponsored by Google since late 2019
- Uses Antlr4 for parser and pre-processor code generation, Capnp for object persistency
- Successfully synthesizes: **BlackParrot, OpenTitan** open-source cores, more to come
- Verified by Yosys Formal Verification against Yosys parser
- 1000s of regression tests, reuses entire regressions from Yosys, Verilator, Icarus…



- Focused on Synthesizable subset, but parses entire language and provides most of Verilog Object Model
- Users include several tinkerers, startups, Google, ZeroAsic
- Current usages: Linter, Language Server, Synthesis, Simulation, Design packager
- Google is using it on large internal SV code base
- Possible developments
  - Verilator front-end (resume previous work)
  - VHDL/Mixed designs
  - RTL security analysis
  - UVM – Design static analysis