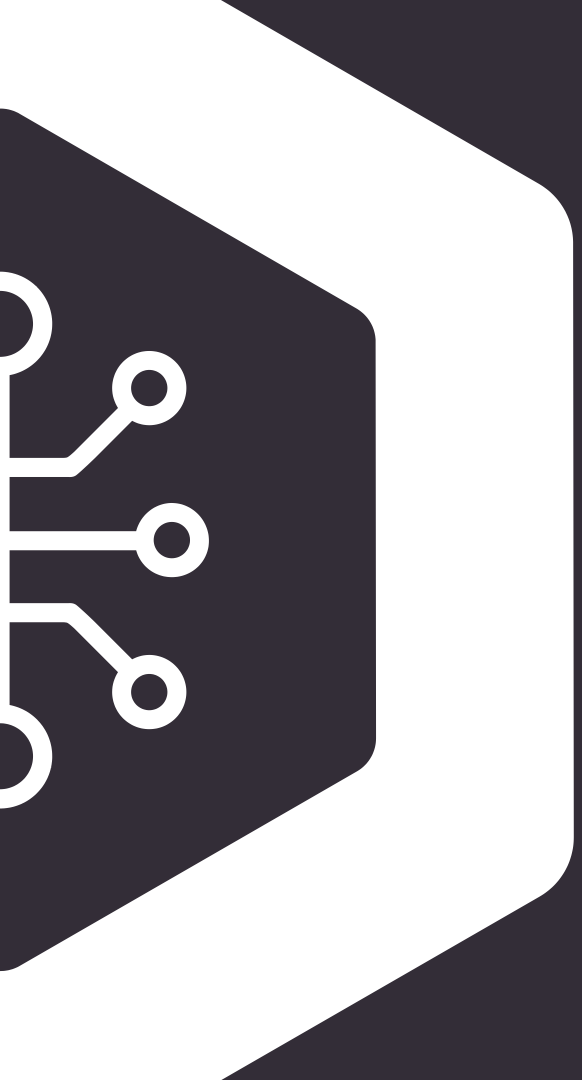

Industry adoption of open source ASIC tools

DAC open source BOF, 2023-07-12

Michael Gielda, mgielda@antmicro.com

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OPEN SOURCE IN CALIPTRA ROT PROJECT @ CHIPS ALLIANCE

- Open source collaboration between Microsoft, AMD, Google, NVIDIA (+ many more)
- Antmicro charged with enabling open source collaboration tools in the project for both current project partners and external adoption
- Took over maintenance of VeeR cores family, Caliptra CI, helping with RISC-V DV
- Productivity tooling and CI
  - Verible, Kythe for formatting, linting, indexing
  - tests with Cocotb, pyUVM, RISC-V DV
  - System-level testing and integration
  - Public-facing CI

VERILATOR SCALING AND OPEN SOURCE VERIFICATION

- Continuing commercial work on debugging, optimization, improving SystemVerilog support
- Learning about new users of event-driven simulation we adder earlier!
- Continuing work on UVM - very close to parsing the entire UVM library (multi-state logic and constrained random still WIP)
- Lots of people at and after RISC-V Summit Barcelona approaching us to either congratulate on the work or request more help

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RENODE ADOPTION AND GROWTH

- More and more users in the wild: Garmin, Toyota, Novo Space, Microsoft, etc. etc.
- new customers in pretty much all industries: automotive, space, logistics, consumer electronics, semicons, robotics, smart energy...
- Covering the entire ARM space: 64-bit Cortex-A, Cortex-R52, starting work on Cortex-R8
- RISC-V continuously improved, more and more heterogeneous SoCs with both ISAs
- DPI support, QuestaSim / Verilator integration
- NB-IoT support, running 300+ nodes, more pre-silicon use cases, TBM, and more