Thermal design as a first-order concern

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Outline

- IC design metrics
- Worst-case vs. adaptive design
- Thermal design knobs
- Architecture/Circuit – ESL/RTL/P&R co-design
- NSF POSE

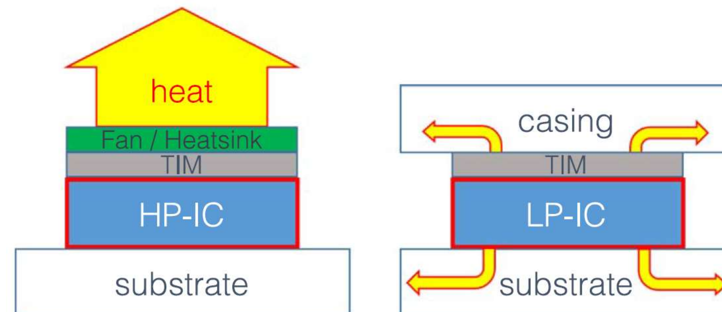
IC design metrics

- A (60's-70's) -> PA (80's-90's) -> PPA (2000's) -> PPAT (2020's)
- (Moore) (Dennard) (Chandrakasan)
- Thermal Design Power (TDP)
- Same silicon/different cooling -> drastically different performance
- 2.5D/3D – dimensional mismatch between power dissipation (volume L^3) and heat removal (area L^2)

Traditional thermal design

- post chip design by a packaging team
- power model typically fixed/steady state (worst case)
- thermal model typically steady-state with or without spatial detail
- IC energy cycle

Electrical energy/power in, heat out

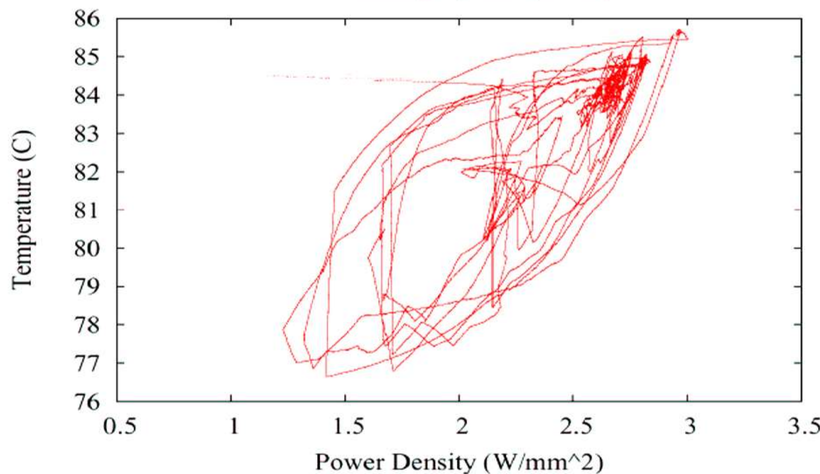


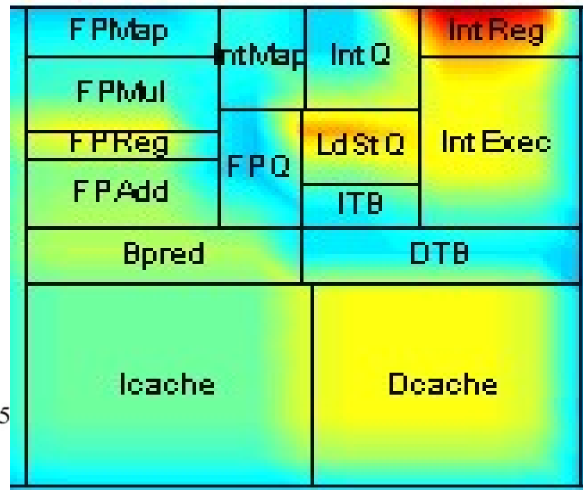
Coudrain, Perceval, et al. "Experimental Insights into Thermal Dissipation in TSV-Based 3D Integrated Circuits." IEEE Design & Test of Computers 1 (2016): 1-1.

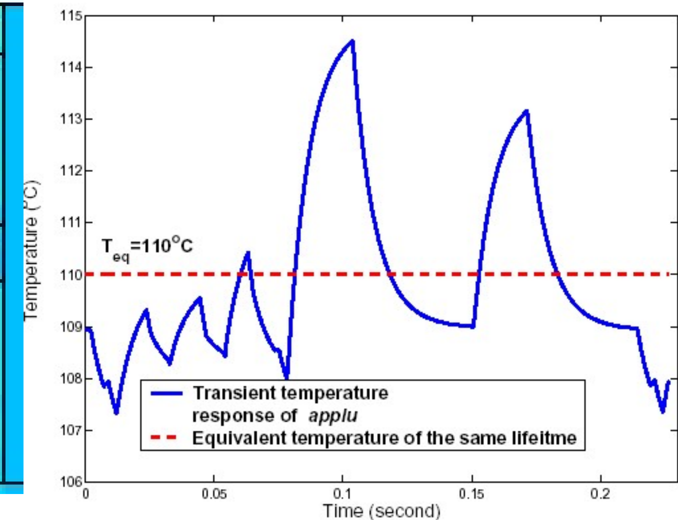
Worst case vs. adaptive design

HotSpot original contributions (20 years ago!):

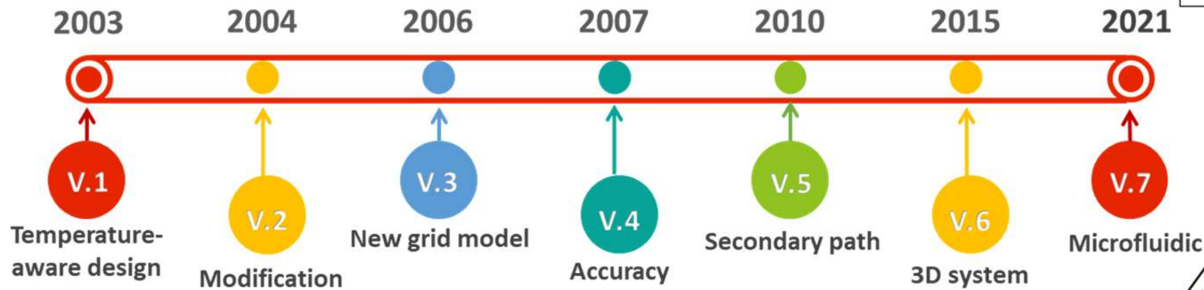
- Power *cannot be used as a direct proxy* for thermals
- Need for thermal models for both *spatial* and *temporal* variations

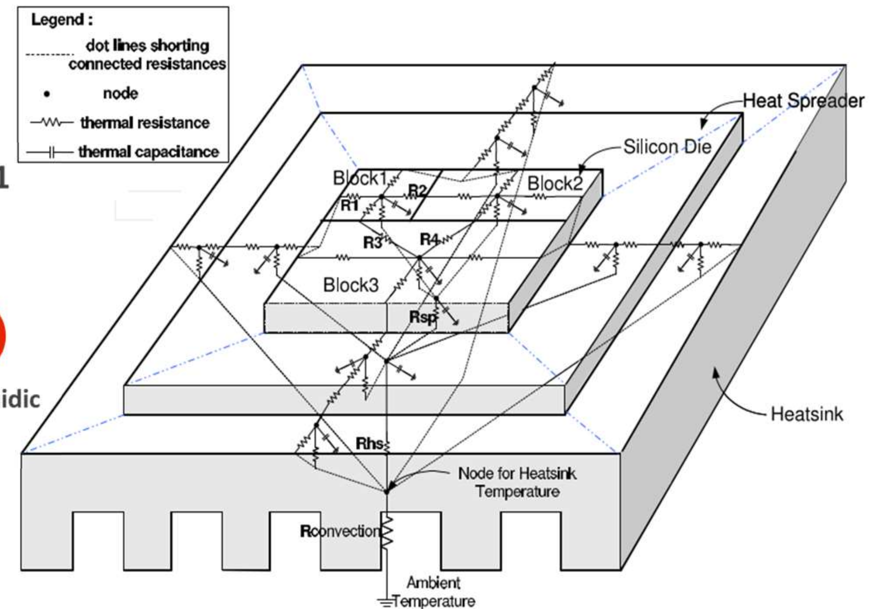


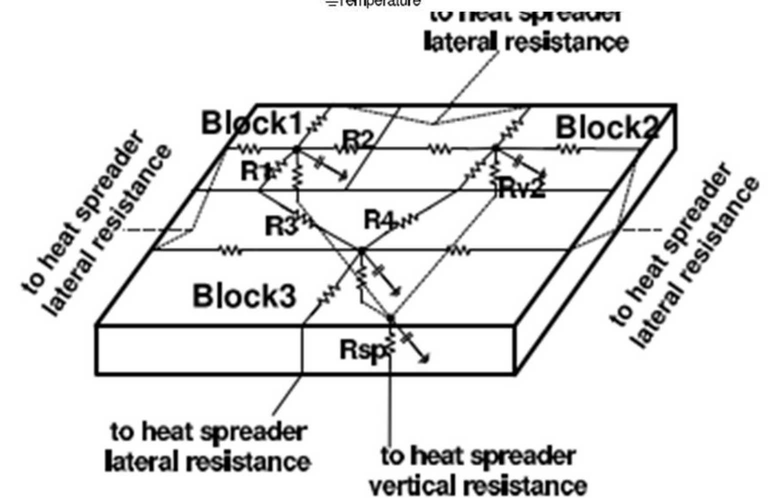




HotSpot





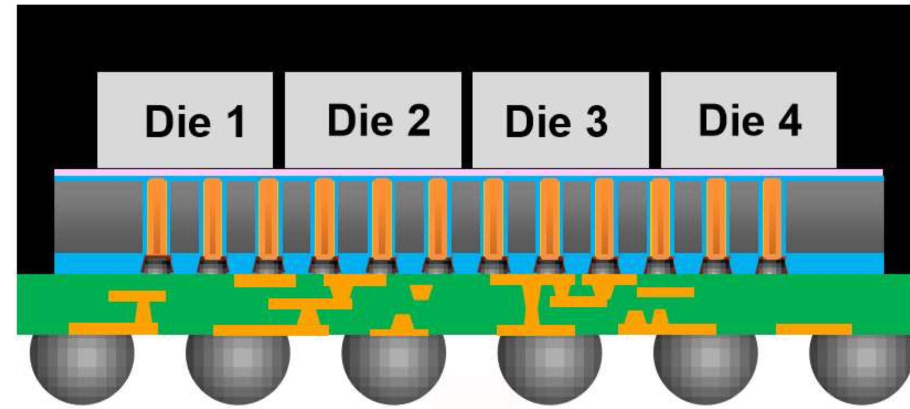


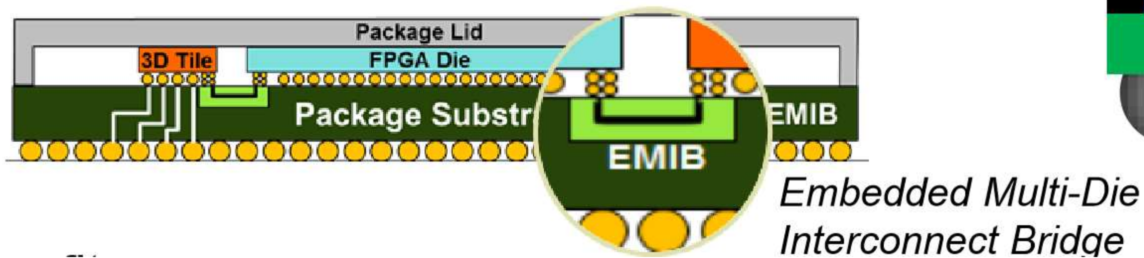
- 1.0 - Original block thermal model
- 2.0 - Grid model, validation test chips, TIM
- 3.0 - Better solvers, die edges
- 4.0 - Better solvers, more accuracy
- 5.0 - Package, secondary path
- 6.0 - Better solver (SuperLU), 3DIC
- 7.0 – Microfluidic cooling

https://github.com/uvahotspot/HotSpot

Recent needs in thermal research – 3DIC

- Interposer vs. EMIB vs. TSV-based 3D
- Different tradeoffs!





Embedded Multi-Die Interconnect Bridge

DRAM Stack

Cadix, Lionel. "2.5D interposer 3DIC and TSV interconnects." *European 3DTSC Summit,* January 2013 (2013).,

Hutton, Mike. "Stratix® 10: 14nm FPGA delivering 1GHz." *Hot Chips 27 Symposium (HCS), 2015 IEEE*. IEEE, 2015.,

Michailos, J., et al. "New challenges and opportunities for 3D Integrations." *Electron Devices Meeting (IEDM), 2015 IEEE International.* IEEE, 2015.

HotSpot 7.0 three circuit abstractions for 3D IC

Electrical Circuit	Models heat dissipation throughout the 3D IC	Voltage	Electric Current Flow	Electrical Resistance
Pressure Circuit	Models the flow of coolant through the microchannels	Pressure	Fluid Flow	Hydraulic Resistance
Thermal Circuit	Models heat transfer throughout the 3D IC	Temperature	Heat Flow	Thermal Resistance

Thermal design knobs

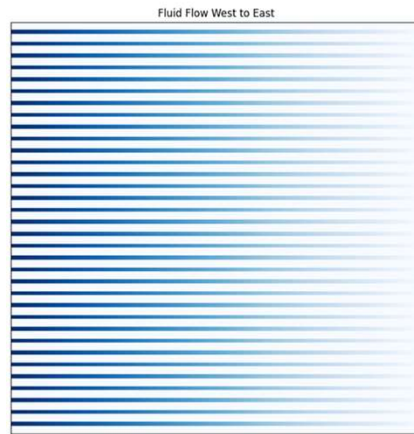
Back to energy cycle:

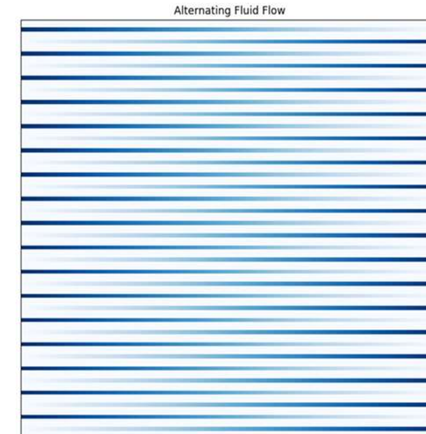
- Adjustable *power model* - spatial and temporal adjustments: dark silicon, migrating computation, big/LITTLE, throttling, DVFS, power modes, etc.
- NEW – Adjustable *thermal model* – spatial and temporal adjustments: fluid flow pattern, fluid flow rate.

From fixed to adjustable thermal model

Intel i7-3960X

Microchannel Flow Direction

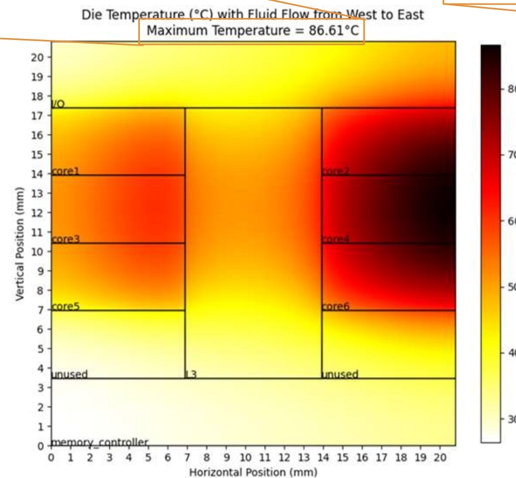


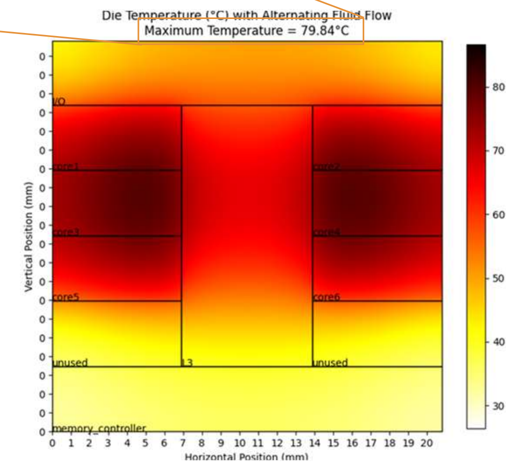


Max. Temperature: 86.61°C

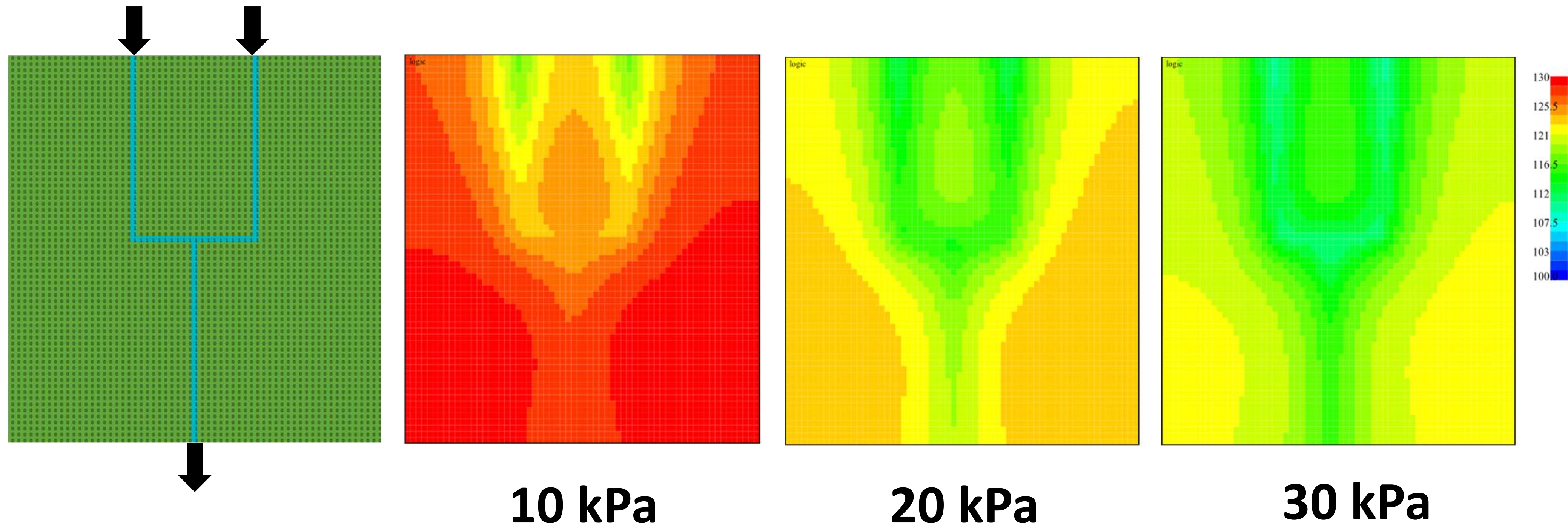
Max. Temperature: 79.84°C

Resulting Heat Map

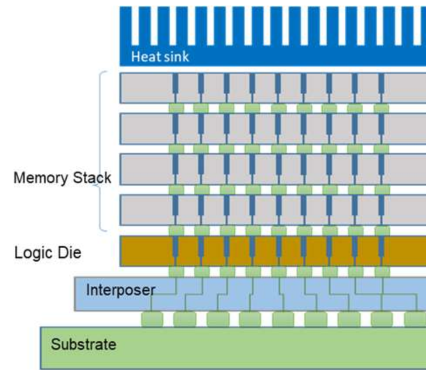


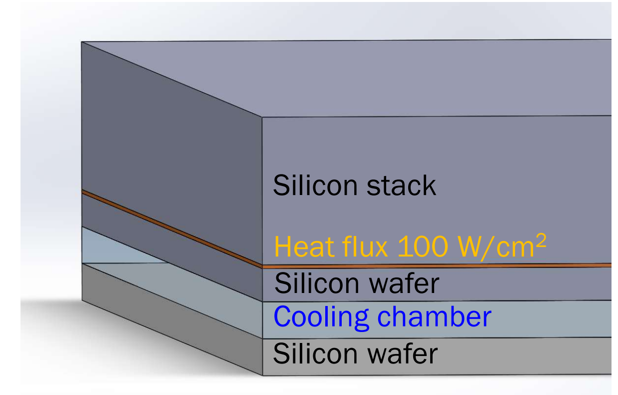


Changing the flow rate (pump pressure)



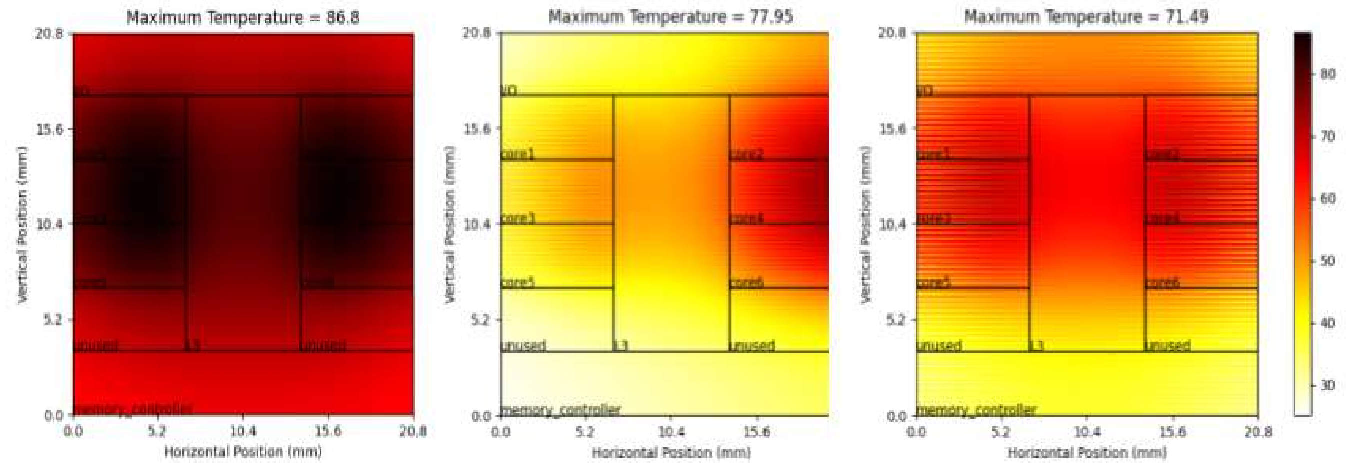
Cooling a 3D PiM





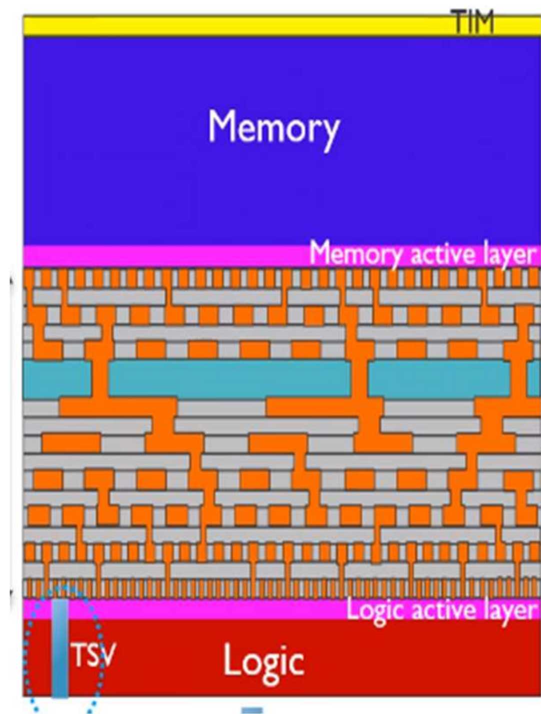
Processing-in-3D-Memory

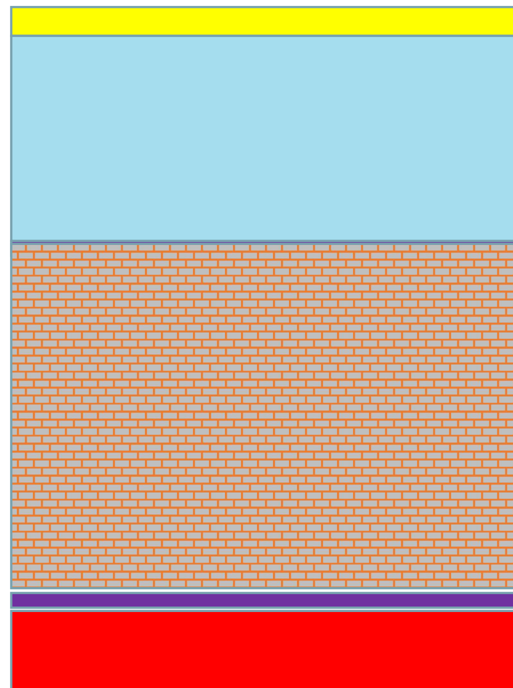
Junhan Han et al. “Thermal Simulation of Processing-in-Memory Devices using HotSpot 7.0”, Therminic 2022

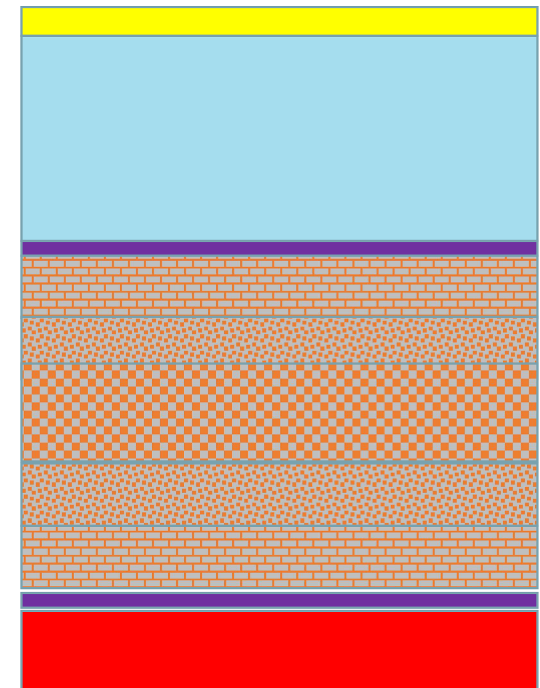


Heat sink, unidirectional flow, alternating flow

BEOL modeling







Architecture/Circuit – ESL/RTL/P&R co-design

- Integration with/expansion of OpenROAD
- Gate-level thermal transient simulation will be too slow
- Need to run architecture-level workloads
- Need to extract thermal models to run pre- and post-RTL
- Need composable models/solvers (Spice?)

NSF POSE

- Pathways to Enable Open-Source Ecosystems (POSE)
- https://new.nsf.gov/funding/opportunities/pathways-enable-open-source-ecosystems-pose
- September 7 2023 - Deadline date
- Phase I: OSE Scoping and Planning Proposals - $300k/1 year
- Phase II: Establishment and Expansion Proposals - $1,500,000/2 years
- Upcoming - July 27, 2023 - Webinar: NSF Pathways to enable Open-Source Ecosystems (POSE)