OpenRAM Open-Silicon
Current Results and Future Plans

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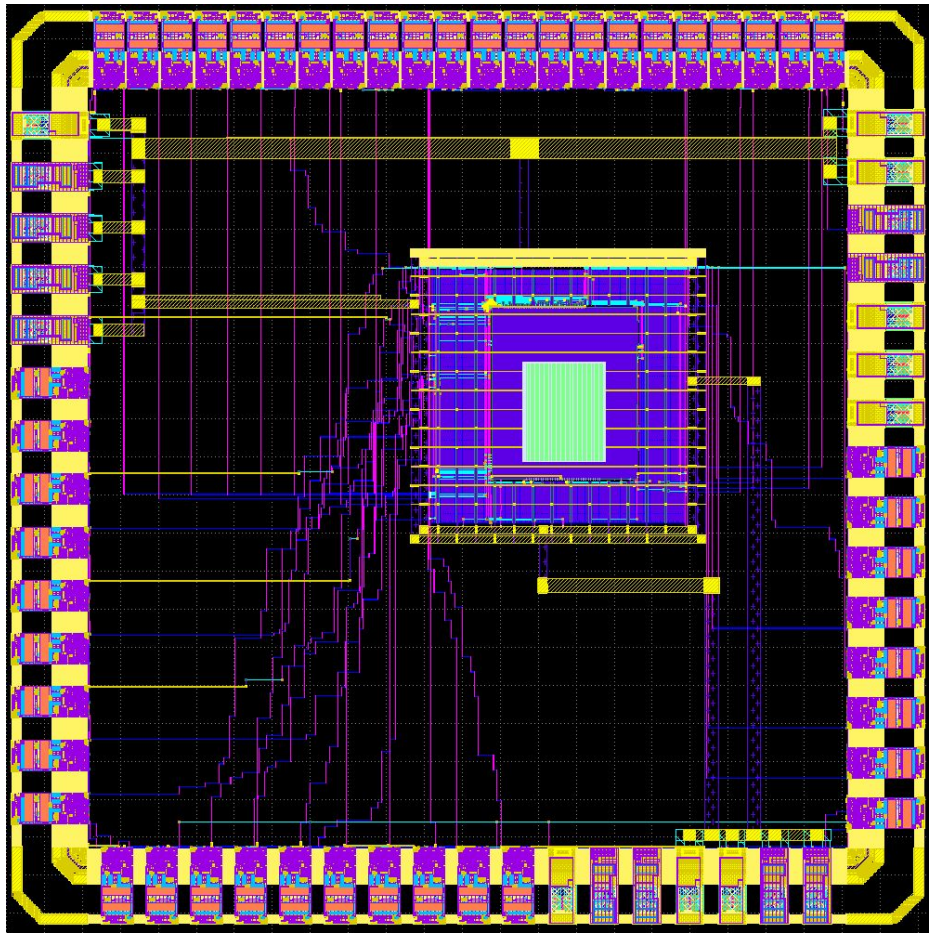
https://github.com/VLSIDA/OpenRAM

TLDR: OpenRAM

- Implemented in Python 3.5+
- Licensed with 3-clause BSD
- Separate front-end and back-end modes
- Provides a fast analytical timing/power characterizer + accurate Spice based character
- Spice based functional verification
- Generates GDSII layout data, SPICE netlist, Verilog model, DRC/LVS verification reports and P&R macro view.
- Wrappers for both open-source and commercial tools

OpenRAM Test-Chip One (OR1)

- 32-bit
- 1kb
- 1RW1R dual port design
- Similar to 2kb dual port macro on the Caravel management core
- Developed with closed source DRC/LVS tooling



OR1 test-chip layout with 1kb dual port SRAM

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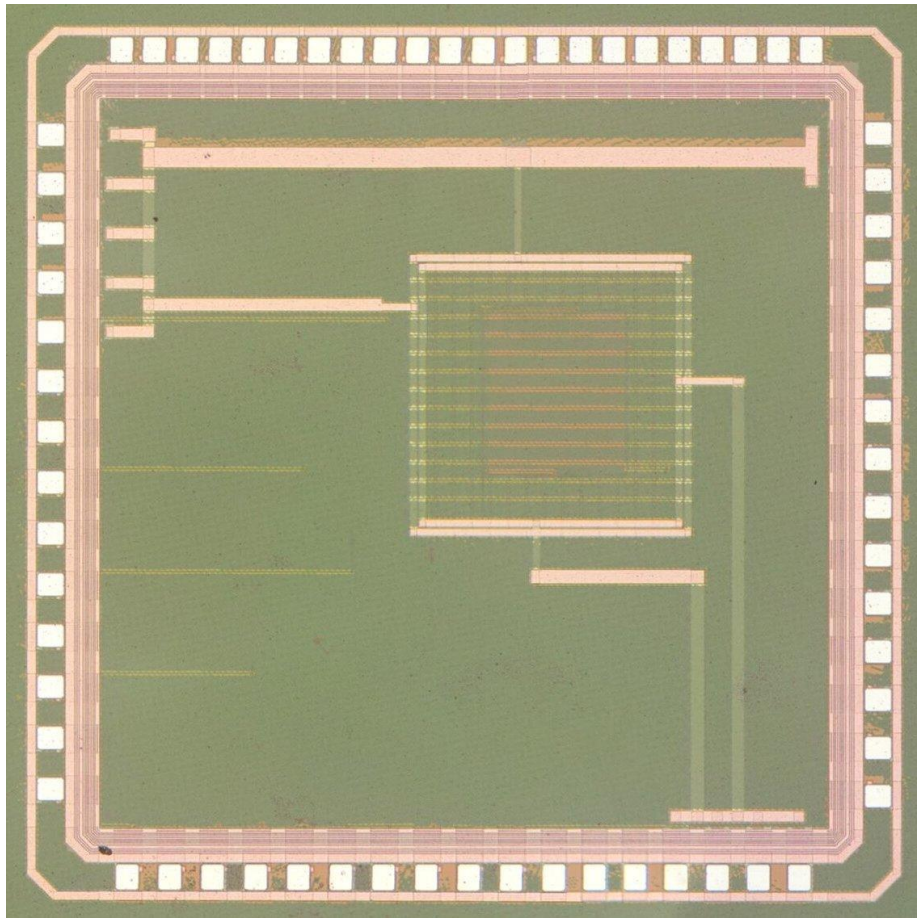
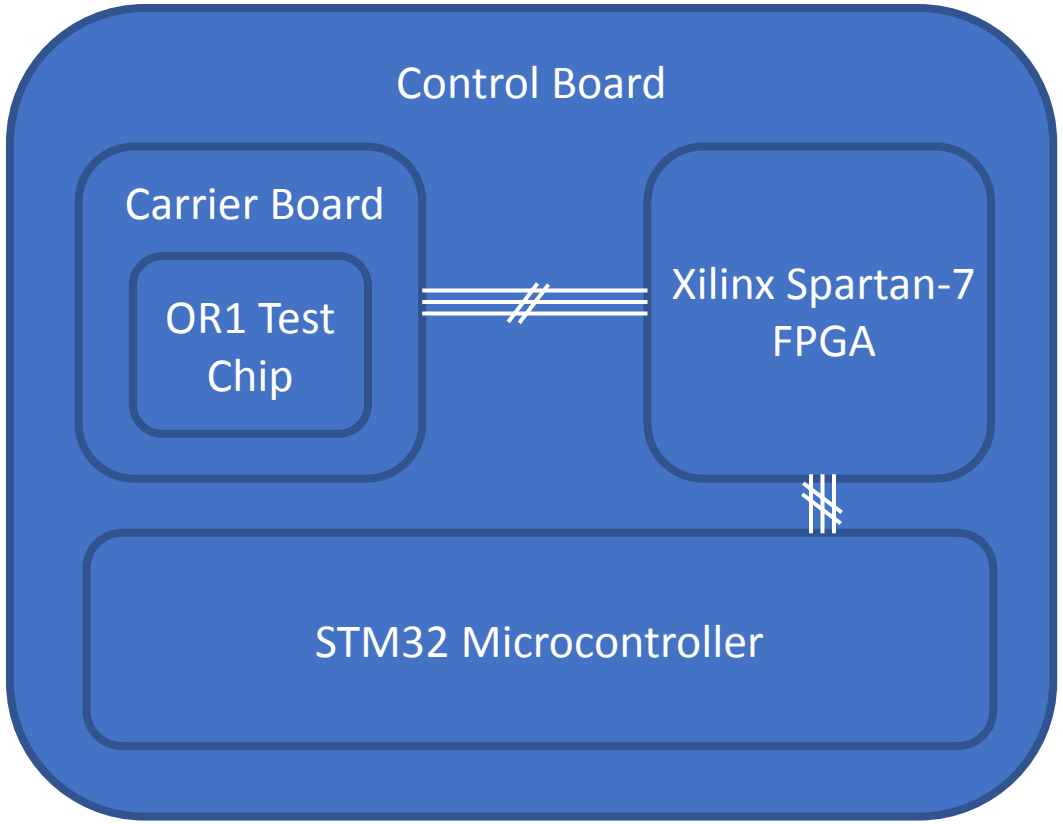
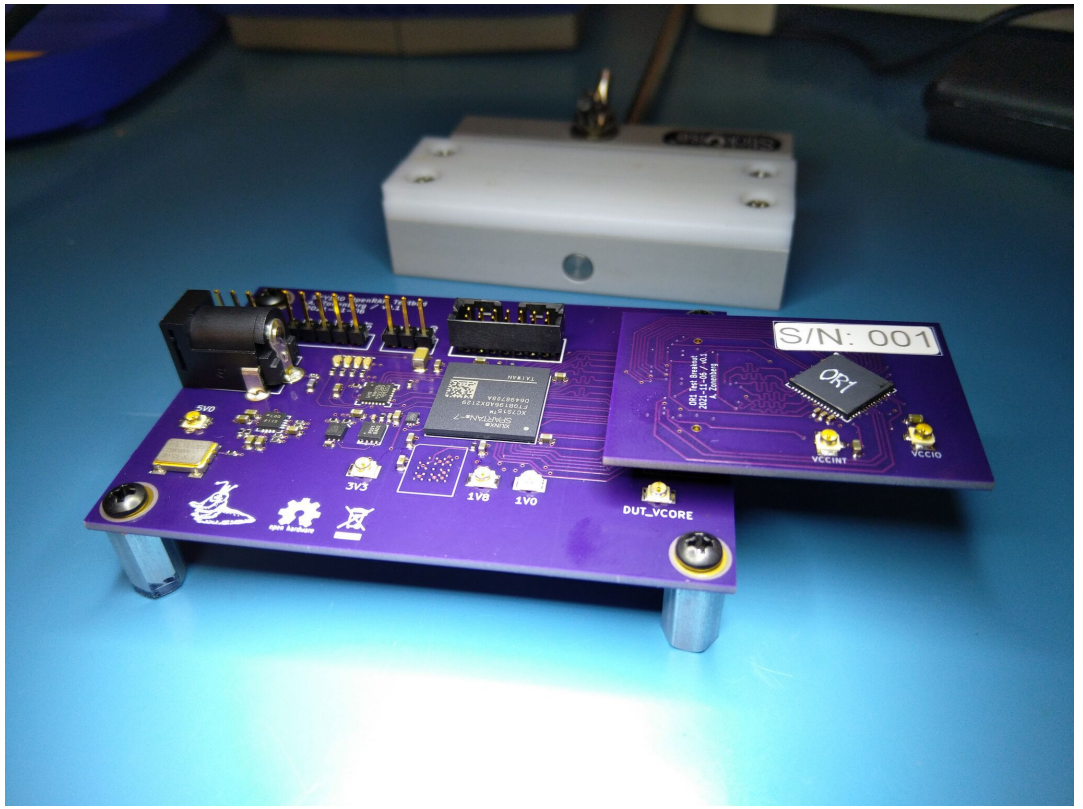
Tapeout – OR1

- Single 32bit 1kb 1RW1R SRAM macro
- SRAM control bonded out directly to I/O
  - Clock, chip select, write enable, and write mask signals
- Limited I/O so MSB and LSB of each byte (for each port) was bonded out
- Manual creation of SRAM macro power rings
- Inputs DFFs but no output DFFs



Test and Measurement – OR1





Designed by Andrew D. Zonenberg

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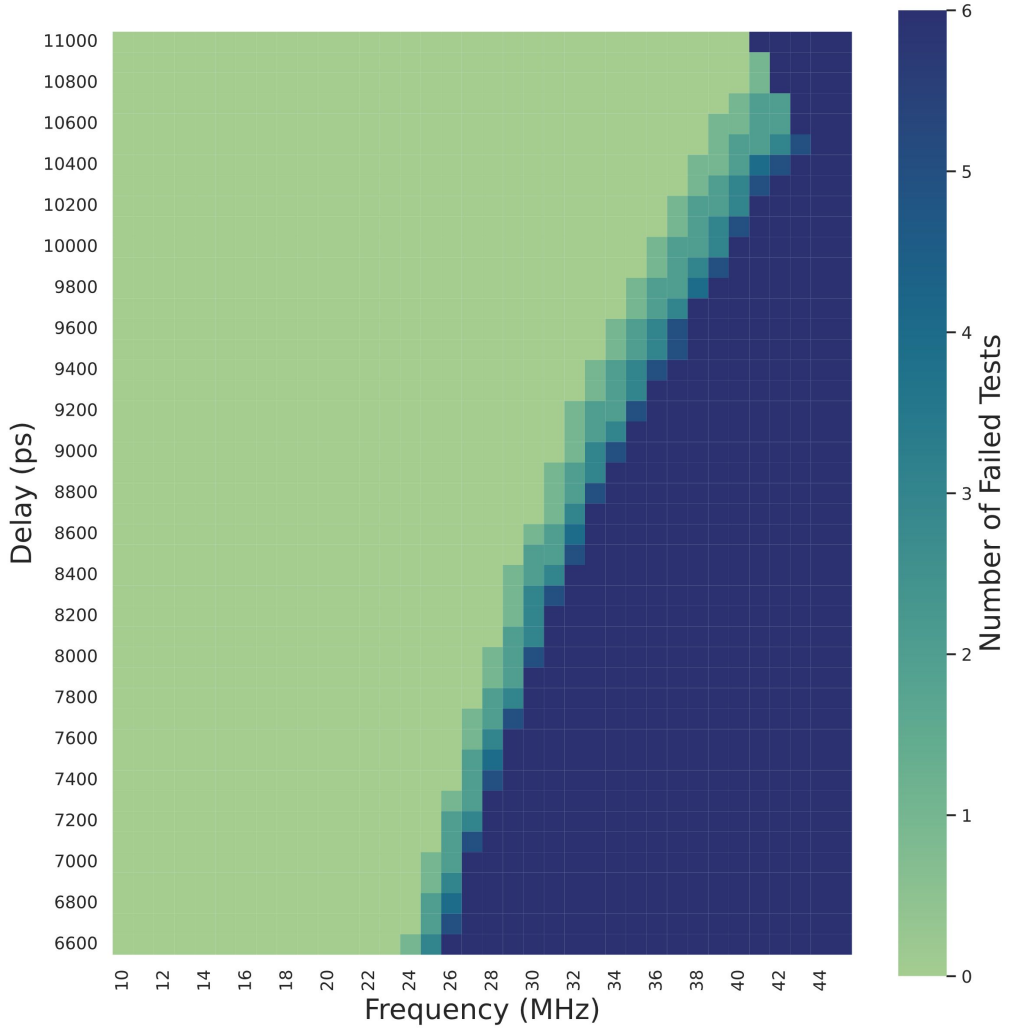
Read Capture Delay vs Frequency – OR1

- Each point is tested for single and dual port operation at three different temperatures for 6 total tests
- Swept from 10Mhz to 44Mhz, 6.6ns to 11ns capture delay
- 6.6ns min capture delay at 23Mhz
- 11ns min capture delay at 39Mhz



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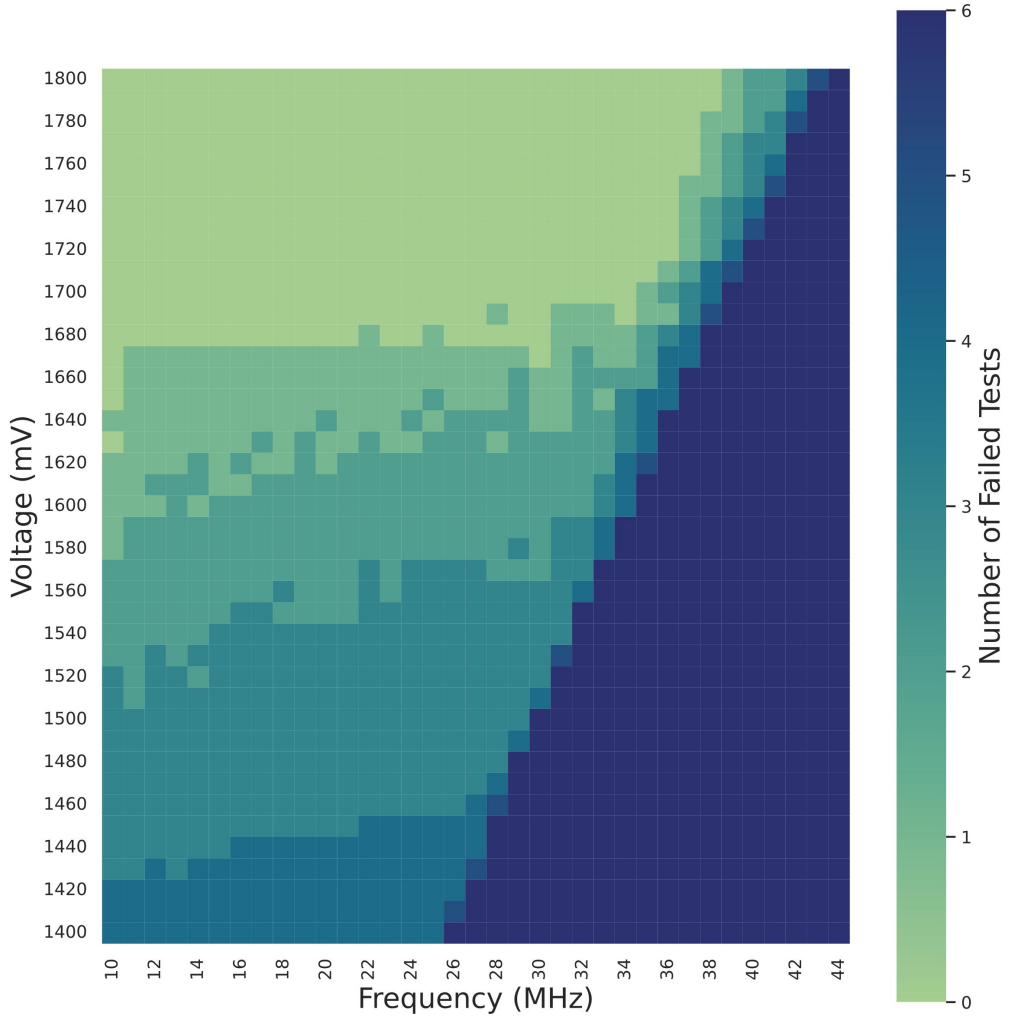
Operating Voltage vs Frequency – OR1

- Swept from 1.4V to 1.8V and 10 Mhz to 44Mhz
- No errors below 34Mhz at 1.7V
- For a single read port there are no errors below 25Mhz at 1.54V



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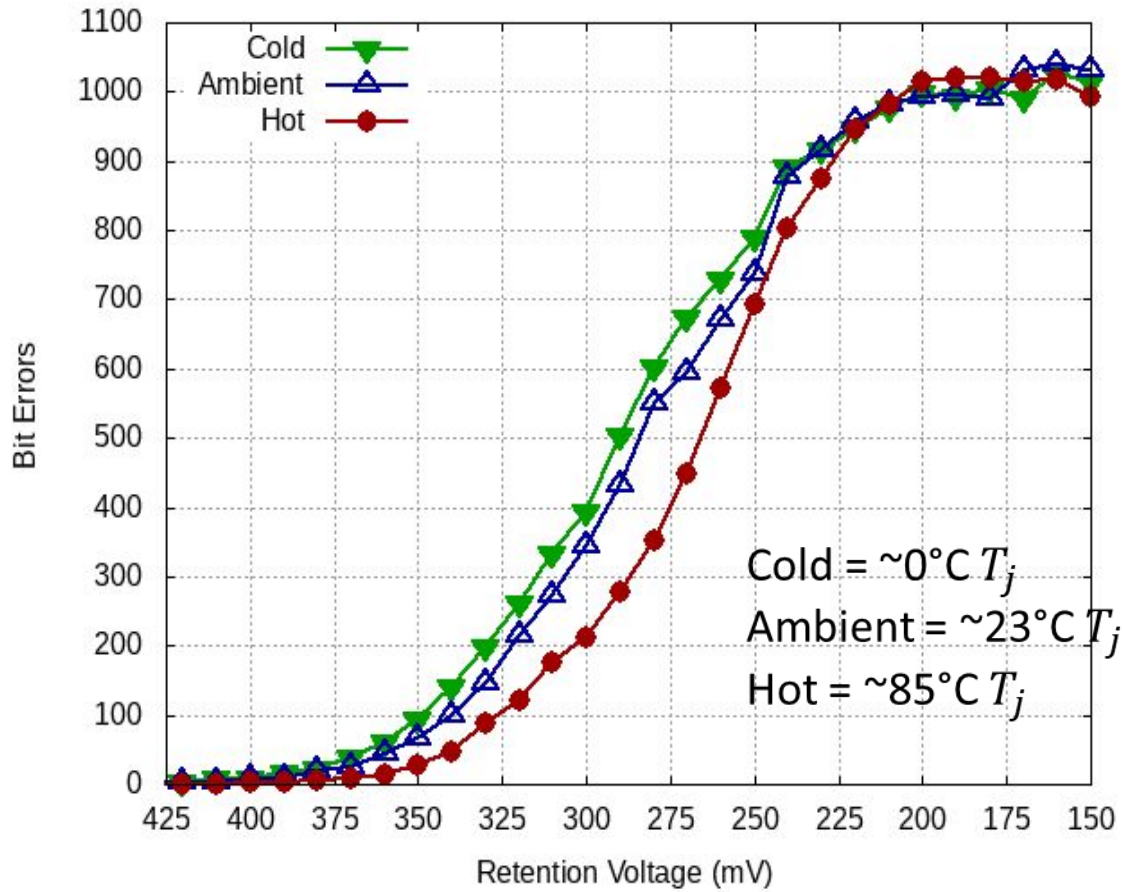
Bit Errors vs Retention Voltage – OR1

- First errors are observed at 440mV when cold and 410mV when hot



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Other chips using the 1 kbyte SRAM

FABulous (UK Manchester)

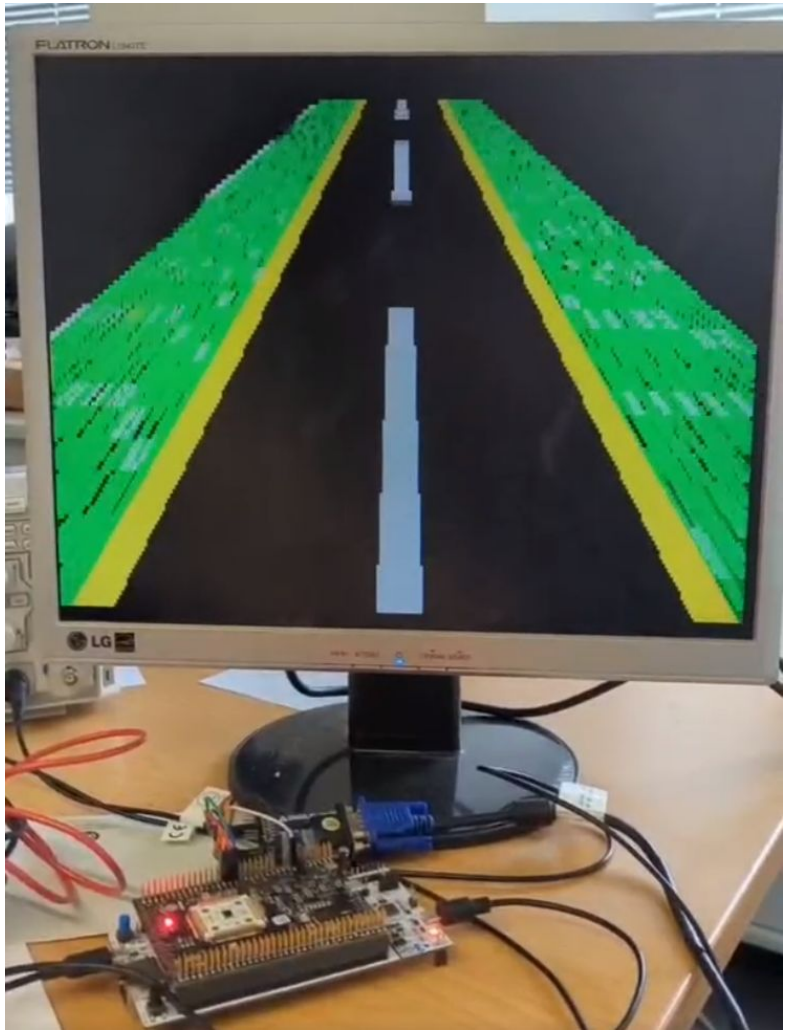
https://github.com/FPGA-Research-Manchester/FABulous

FPGA Fabric with SRAM block RAMs

AHA/Garnet (Stanford)

https://github.com/pohantw/caravel_user_project

CGRA with SRAM block RAMs



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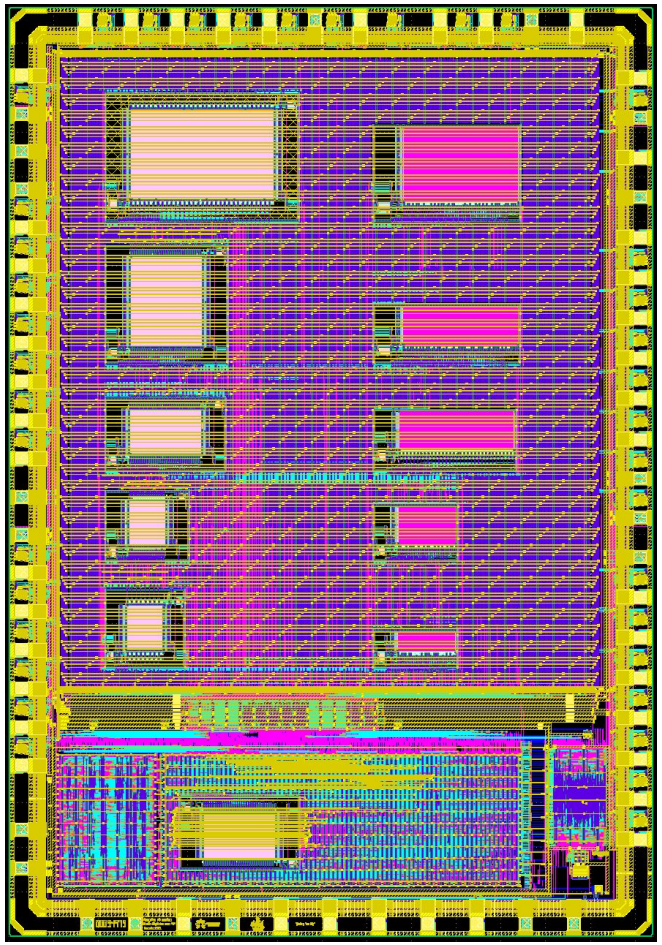
Multi-Project Wafer 2 Test Chip (MPW2)



MPW2 Layout with 10 OpenRAM SRAMs and Caravel management core

- 5 dual port + 5 single port macros
- 1-8kb 32 bit 1RW1R macros
- 1-8kb 32/64 bit 1RW macros
- Developed with entirely with open-source tools!

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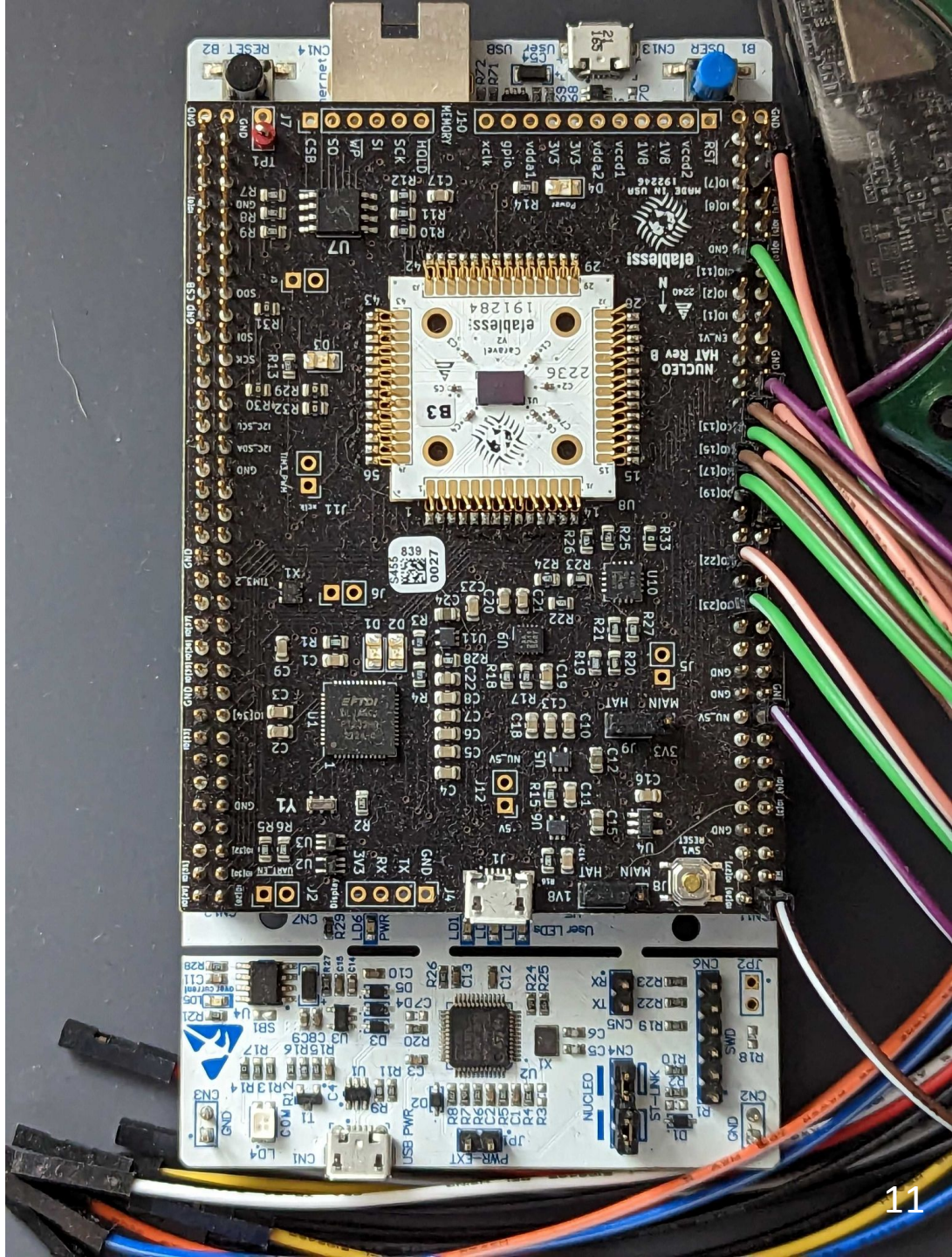
Tapeout – MPW2

- 5 single and 5 dual port SRAM macros
- Parallel on chip logic analyzer + GPIO for testing
- On-chip clock with off-chip backup
- Custom signal escape router for automatic routing of signals to macro perimeter
  - Enables compatibility with OpenLane Triton Route
- Power rings around memory and metal blocking LEF view
  - Enables compatibility with OpenLane power distribution network router



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Test and Measurement – MPW2

- Status
  - Two of 8 test dies can have the GPIO programmed at 1.4V
  - OpenRAM test-chip scan chain not responsive at 1.4V
  - Re-ran STA with new extraction and no significant setup/hold problems
- To-Do
  - Re-run STA with updated SRAM lib models
  - Working on reconfiguring LDO from 1.4 -> 1.8V after GPIO configure
  - Recreating previous test-benches and simulations on VexRISC instead of PicoRV32

Future Work

- MPW3 received as well
- Updating SRAM Liberty models
  - Previous models underestimated setup/hold times due to internal clock skew
  - Stand-alone characterization
- Updating OpenRAM
  - New non-replica bitline control logic
  - Added output isolation buffer
  - Re-factored bit-cell array classes to be more extensible
  - Unregistered inputs + latched output option
- Global Foundries 180nm
  - Underway with basic arrays, but a lot to do
  - Only have 5V/6V bitcell and not 3.3V
- **Challenge: Not enough help!**