efabless.com

CONNECT
COLLABORATE
CREATE

Taping Out Open Source Silicon in Practice

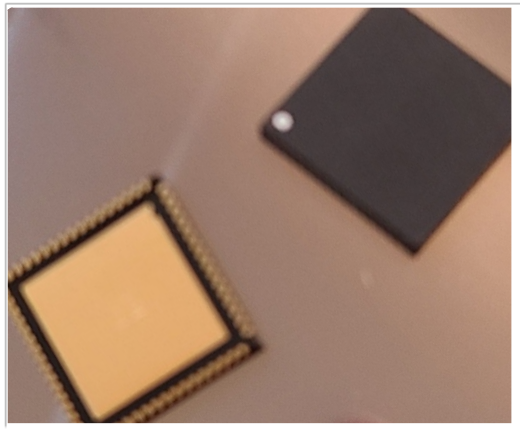
From 1st Principles to AI assisted tapeout in 285 days.

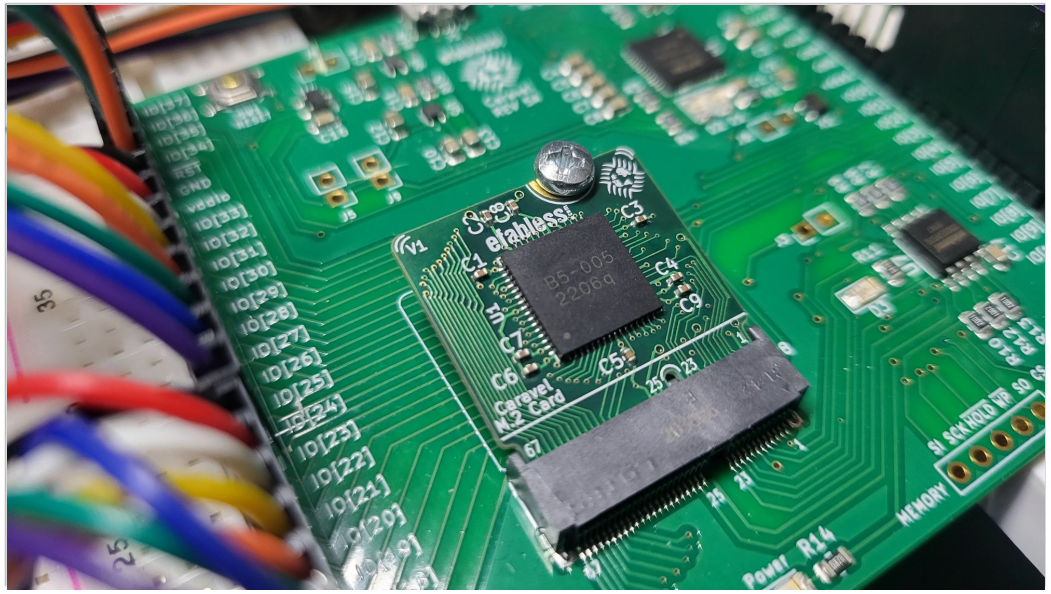
DAC July 12th '23 Birds-of-a-Feather.
Andy Wright

What we do

Simplify the process of **Chip creation** and open it **to Everyone**

Tapeout and Silicon Bringup add learning for all



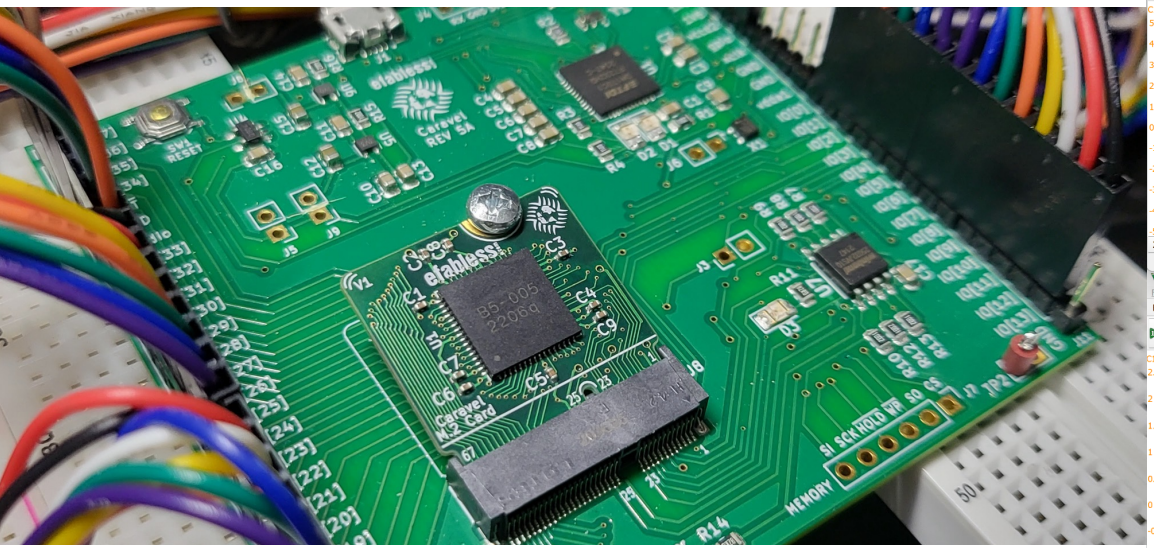


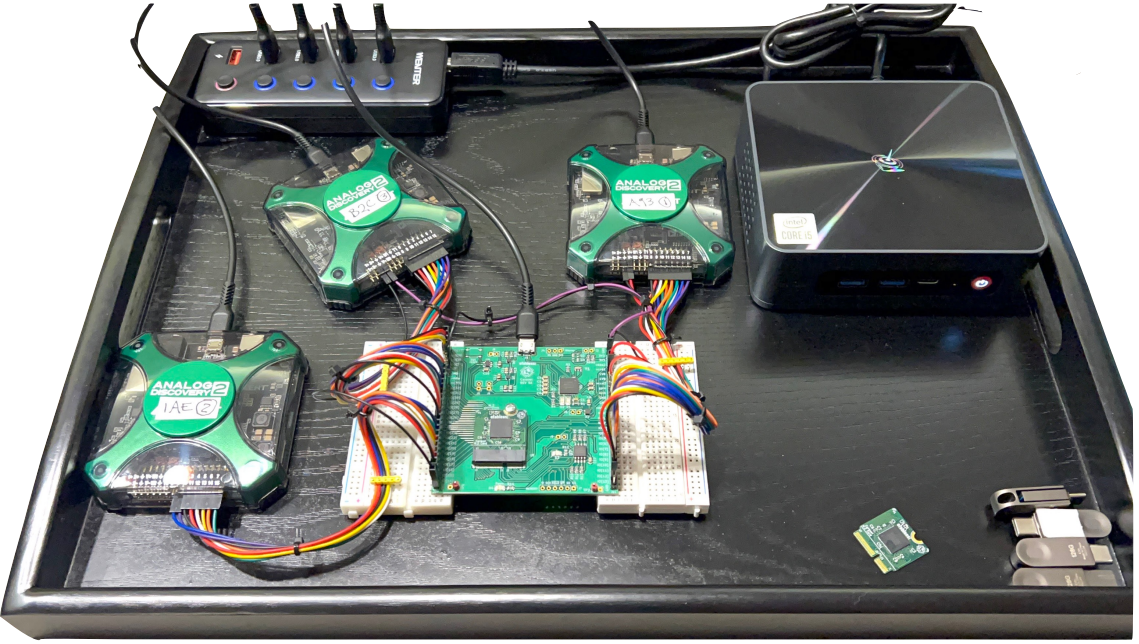
Designers receive packaged chips and assembled evaluation boards for each project

On-chip open source test framework with firmware to support the following:

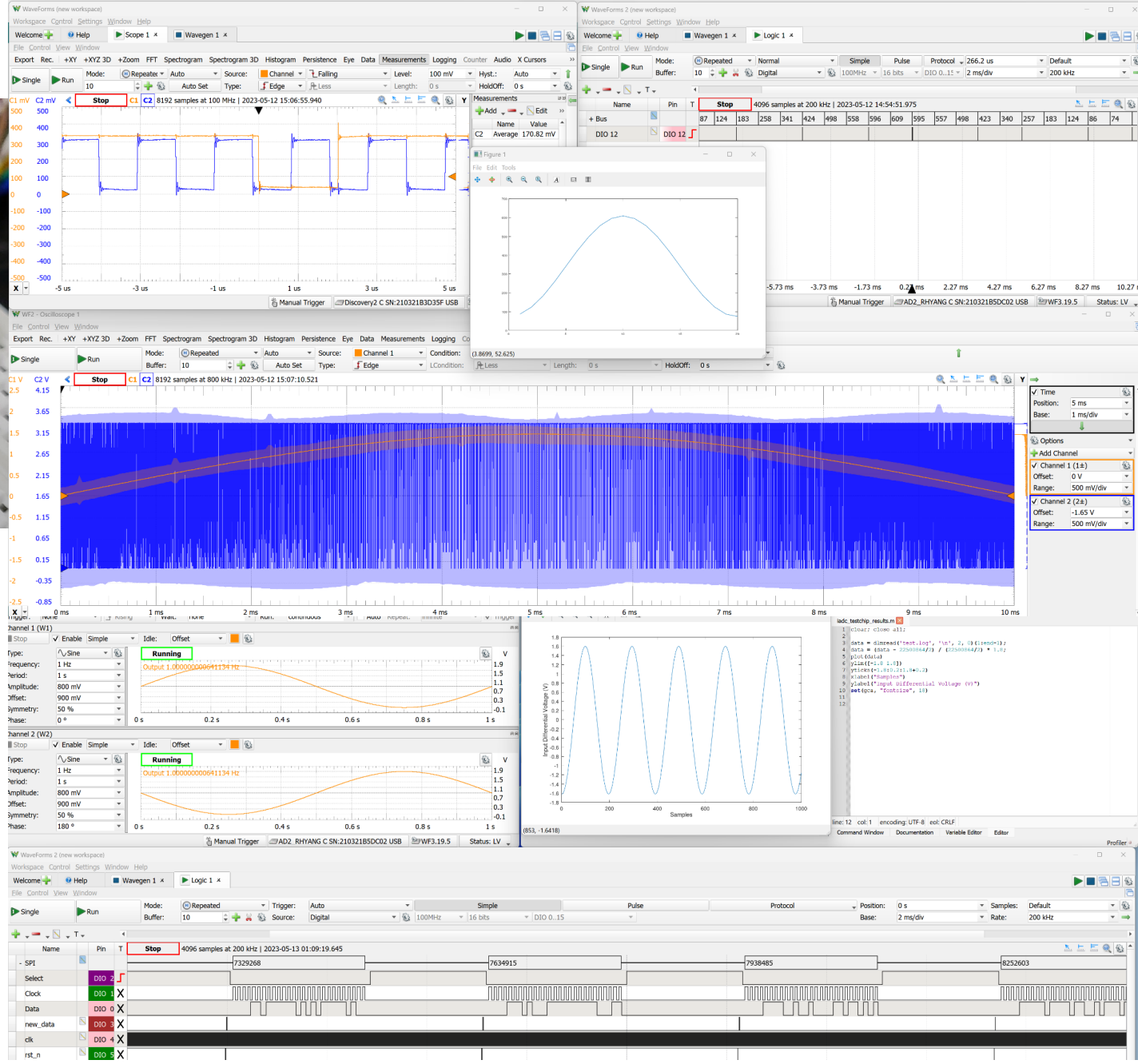
- On-chip logic Analyzer
- Drivers for common peripherals
- Flash memory programming software utility
- Example firmware routines for common functions
- Instructions for customizing firmware for each project

M.2 Development Board





Automated Bench Validation Setup

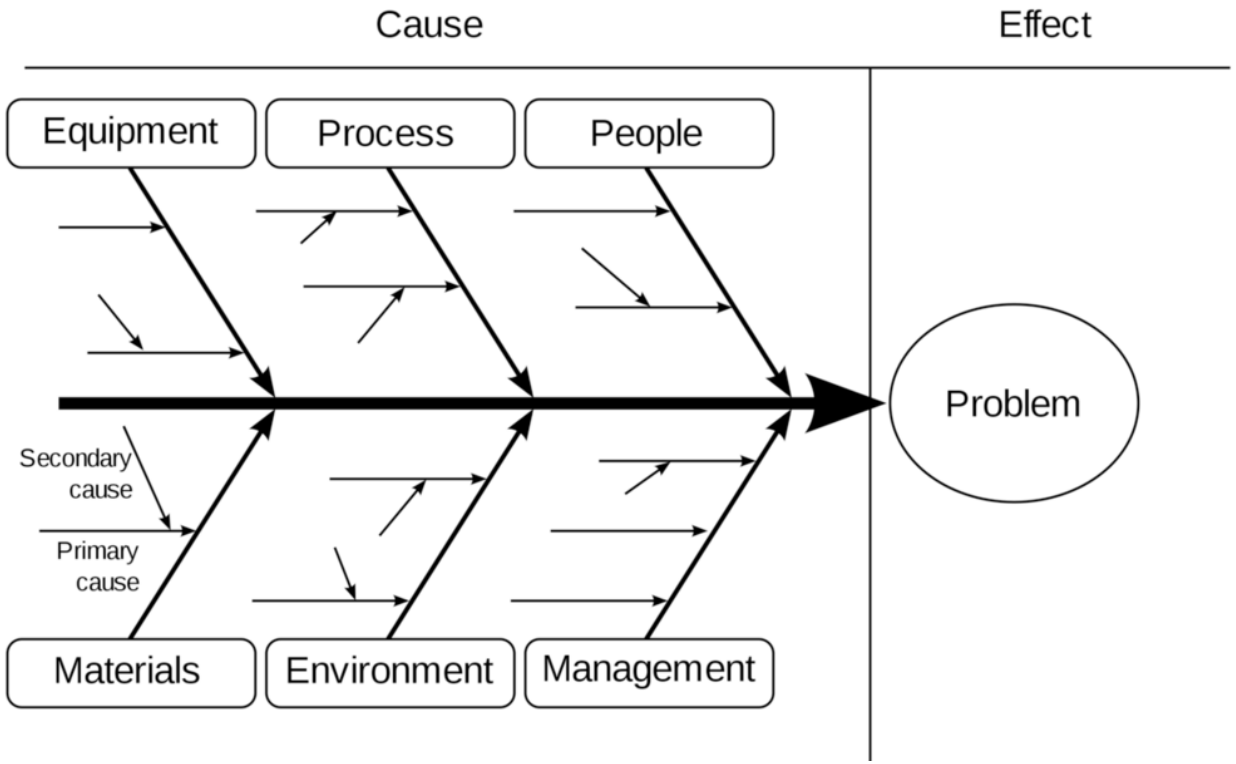


Incremental Delta-Sigma ADC Test Results

Cleanup on Aisle 6

Things went wrong on MPW1-5 before the issues were addressed
Used initially A3 and later full 8D to attack the issues

Equipment remains unchanged
Process, checklist and automation
Staff were added
Design management reviews
Environment was modified
Address rate of incoming change
Materials were added



Results:
1st Silicon success on SKY130 and GF180 in May and June of 2023

For more info: https://www.youtube.com/watch?v=F377UouYr7Y

Caravel Silicon Validation - SKY130

All functional tests meet what's spec'ed

For more information on the bringup watch this

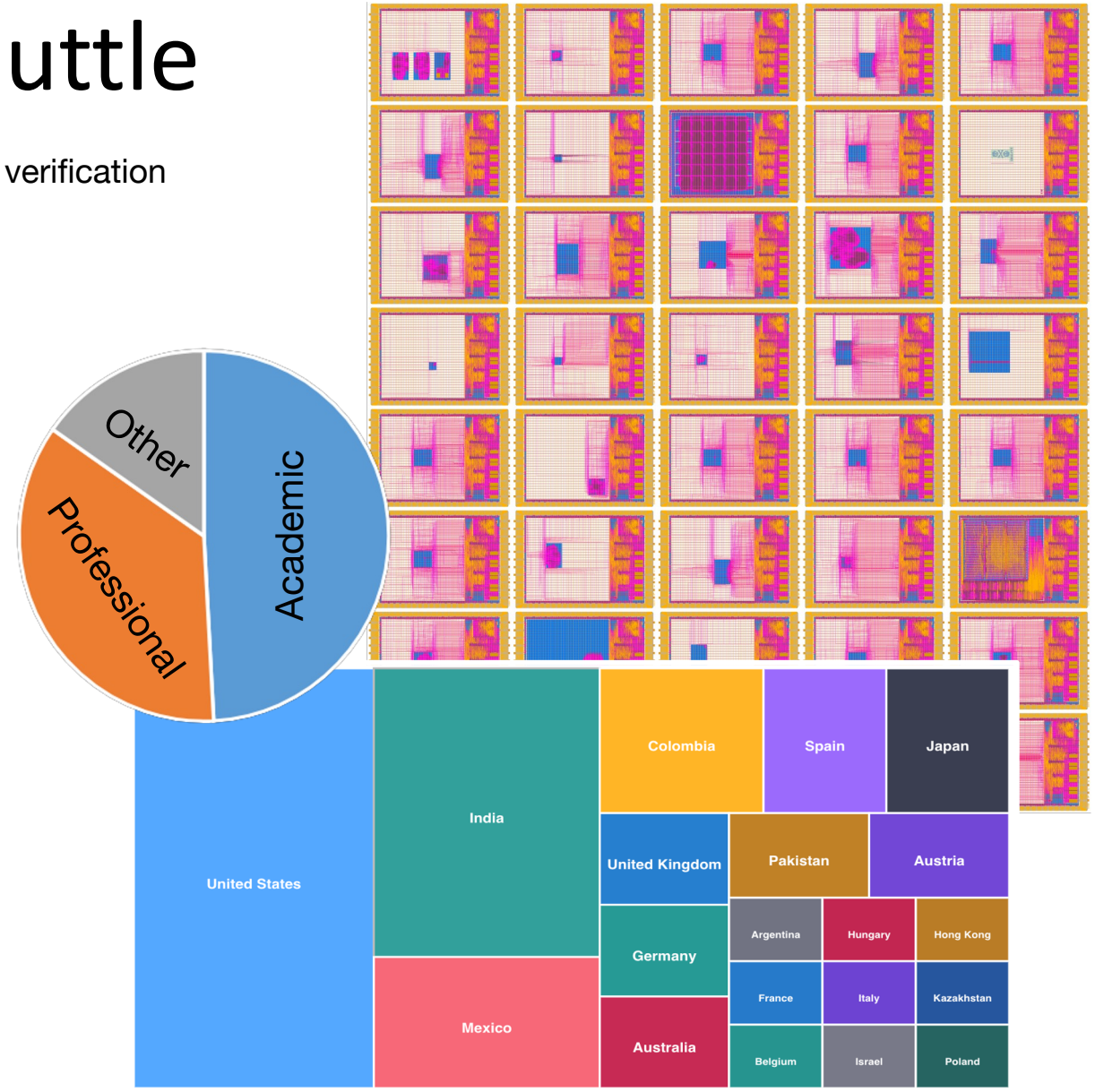
For the full details on the issues watch this

48hrs from wafer-out to fully automated bench validation

Test	SI Valid.	State	1.98v	1.90v	1.85v	1.80v	1.75v	1.70v	1.65v	1.62v
cpu_stress	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
IRQ_external	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
IRQ_timer	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
IRQ_uart	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
IRQ_spi	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
timer0_oneshot	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
timer0_periodic	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
uart_loopback	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
uart_reception	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
uart	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
send_packet	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
spi_master	Yes	Coded	manual	manual	manual	manual	manual	manual	manual	manual
mem_dff_test	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
mem_dff2_test	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
mem_dff_halfw	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
mem_dff2_halfw	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
mem_dff_w	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
mem_dff2_w	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
gpio_o_l	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
gpio_o_h	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
gpio_i_l	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed
gpio_i_h	Yes	Coded	passed	passed	passed	passed	passed	passed	passed	passed

GF180MCU OpenMPW Shuttle

- First shuttle run as a beta with new tools, Caravel design, EDA, verification and tapeout flows
  - **5 weeks** + 2 days for submission
- Timeline
  - Open: October 31, 2022
  - Closed: December 5, 2022
  - GDS in: December 12, 2022
  - Wafer Received: May 5, 2023
  - Validation Complete: May 19, 2023
  - Planned User Shipments: June 26, 2023
- Oversubscribed -- **86 projects** submitted
  - Global participation across 20 countries
  - Design types: MCU, FPGA, Games, Memory, Sensor, Clock, PWM, Test circuits
- Validation completed successfully for Caravel design



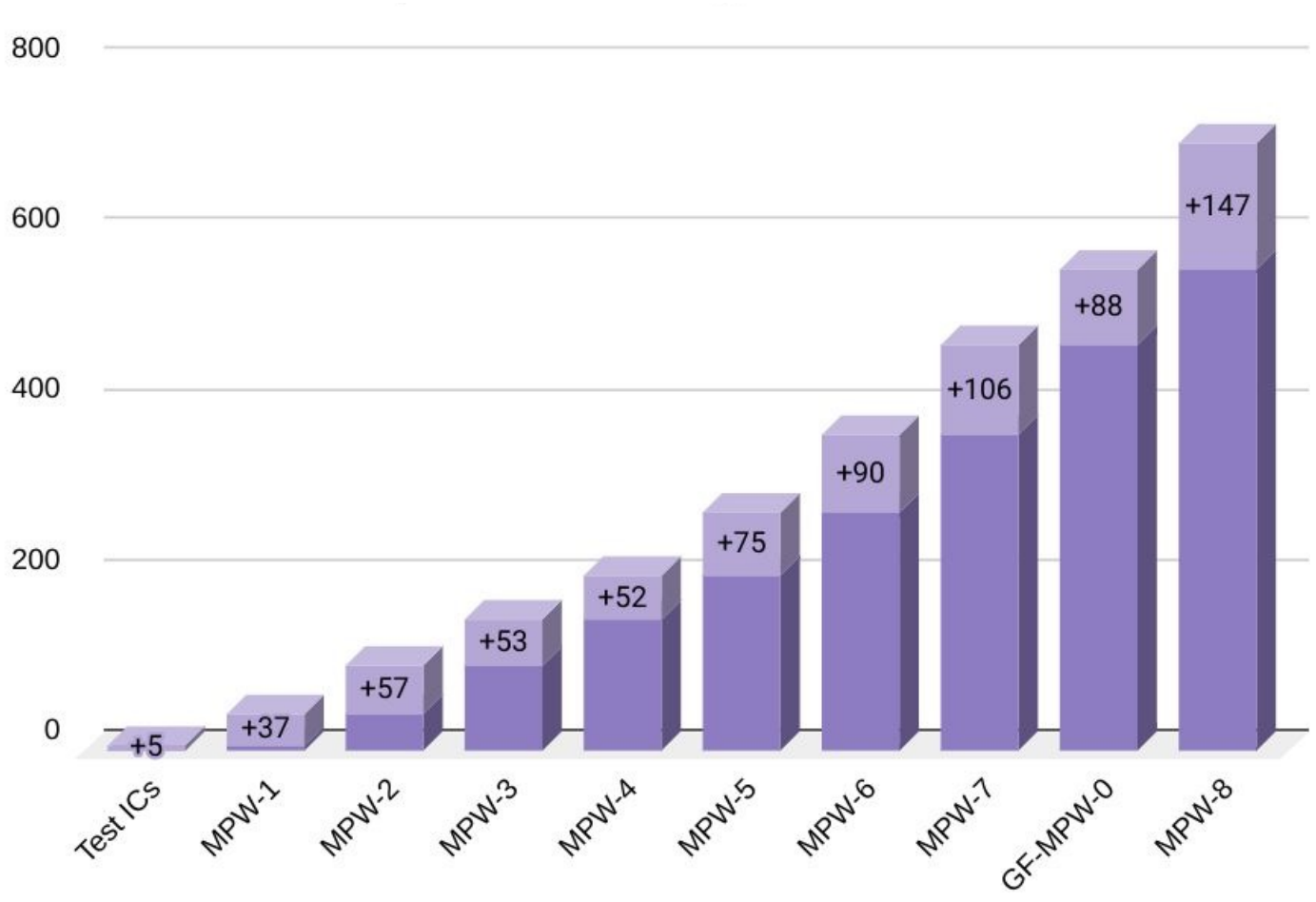
Caravel Silicon Validation

GF180MCU

- GF180 MCU Silicon Works
- 100% tests passing regressions
- 2 run with manual verification
    - constrained by Test HW and will drop from regression

Test	description	SI Valid.	State	5.00v
cpu_stress	Stress the cpu with heavy processing	Yes	Coded	passed
IRQ_external	Test the interrupt from I/O 7	Yes	Coded	passed
IRQ_external2	Test the interrupt from I/O 12	Yes	Coded	passed
IRQ_uart_rx	Test UART rx interrupt	Yes	Coded	passed
IRQ_timer	Test timer interrupt	Yes	Coded	passed
IRQ_uart	Test UART transmission interrupt	Yes	Coded	passed
IRQ_spi	Test SPI with interrupt	Yes	Coded	passed
timer0_oneshot	Timer 0 in one shot mode	Yes	Coded	passed
timer0_periodic	Timer 0 in one periodic mode	Yes	Coded	passed
uart_loopback	UART loop-back test	Yes	Coded	passed
uart_reception	UART Receiption test	Yes	Coded	passed
uart	UART transmission test	Yes	Coded	passed
send_packet	Send random packets through mgmt_gpio to	Yes	Coded	passed
receive packet	Receive random packets through mgmt_gpio to	Yes	Coded	passed
spi_master	Write/Read random addresses from external	Yes	Coded	Manual
mem_sram_test	Test access all bytes of SRAM1 memory	Yes	Coded	passed
mem_sram2_test	Test access all bytes of SRAM	Yes	Coded	passed
mem_sram_halfw	Test access all half words of SRAM1 memory	Yes	Coded	passed
mem_sram2_halfw	Test access all half words of SRAM	Yes	Coded	passed
mem_sram_w	Test access all words of SRAM1 memory	Yes	Coded	passed
mem_sram2_w	Test access all words of SRAM	Yes	Coded	passed
gpio_o_l	Configure the 19 low gpios as mgmt output	Yes	Coded	passed
gpio_o_h	Configure the 19 high gpios as mgmt output	Yes	Coded	passed
gpio_i_l	Configure the 19 low gpios as mgmt input	Yes	Coded	passed
gpio_i_h	Configure the 19 high gpios as mgmt input	Yes	Coded	passed
hk_regs_wr_wb_cpu	write and read housekeeping regs using firmware	Yes	Coded	passed
clock_redirect	redirect caravel clock and user clock on caravel	Yes	Coded	Manual
gpio_lpu_ho	Configure left chain as pull up and map value to	Yes	Coded	passed
gpio_lo_hpu	Configure right chain as pull up and map value to	Yes	Coded	passed
gpio_lo_hpd	Configure left chain as pull down and map value	Yes	Coded	passed
gpio_lpd_ho	Configure right chain as pull down and map value	Yes	Coded	passed

Efabless April ‘21 to Present



0 - 474 Tape-Outs
In 2 Years!

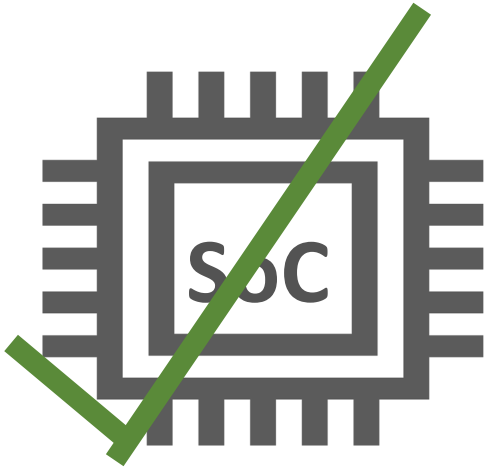
114 chipIgnite
360 OpenMPW

>960 designs created
Pace is accelerating

We can walk. Now what does it take to run?

1. **Market Access** — Open Online Marketplace for Chips Like the App Store
2. **Expertise** — Open Community Collaboration Clusters of global teams
3. **IP** — No NDA or Access Fee Open Source or Obfuscated
4. **EDA Tools** — No Licensing Cost = Open Source Low Licensing Cost = Cloud-based
5. **PDK** — No NDA = Open Source or Obfuscated to protect IP
6. **AFFORDABLE MFG/ASSY/TEST** — No NDA = Open Source or Obfuscated to protect IP while enabling aggregated masks
7. **Bringup Tools** — No NDA = Open Source HW And Automation
8. **Dev Tools** — No NDA = Open Source SW FW dev and verification environment
9. **SOC Platform** — No NDA = Open Source or Obfuscated to protect IP

Solve **1** at time



CAN BUILD USEFUL **CHIPS**

Abstract Complexity
Fast Development
Inexpensive R&D

What is possible today:

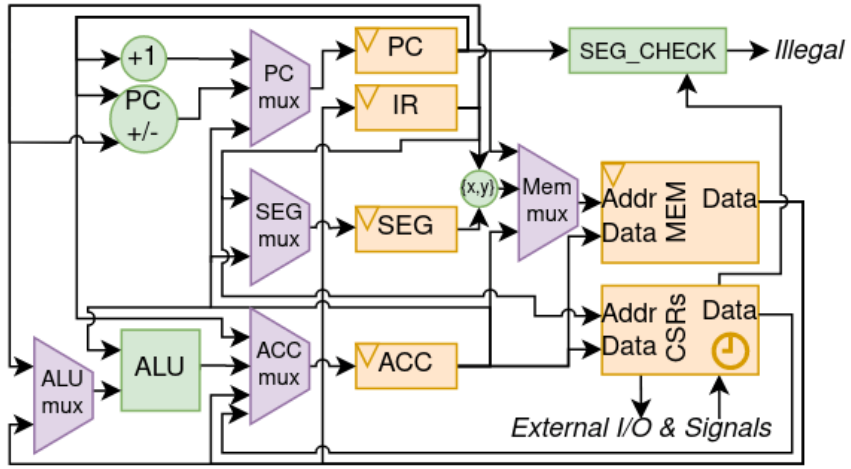
Efabless AI Generated Open-Source Silicon Design Challenge:

"AI combined with the Efabless process is a tremendous enabler for producing custom silicon." Dr. Hammond Pearce

Deadline Final Submissions	6
Submissions Passing Tapeout Pre-Check	6
Previous Open Lane or Caravel Users	1

Concept to Tapeout with 1 person in less than 3 weeks.
In a new tool flow on an unfamiliar PDK using only Open Source tools.

Announced May 19th '23
Final deadline for Submissions June 3rd'23
6 small teams of (1-5 ppl) submitted designs
5 teams had never taped out on Caravel or Openlane
Starting from scratch on a new design after the announcement



https://efabless.com/ai-generated-design-contest
https://efabless.com/hammond-first-place-winner
https://github.com/kiwih/qtcore-C1

Thank You to the entire OS Community!

This could not be done without your contribution

Questions?