Building Confidence in Open IC Design

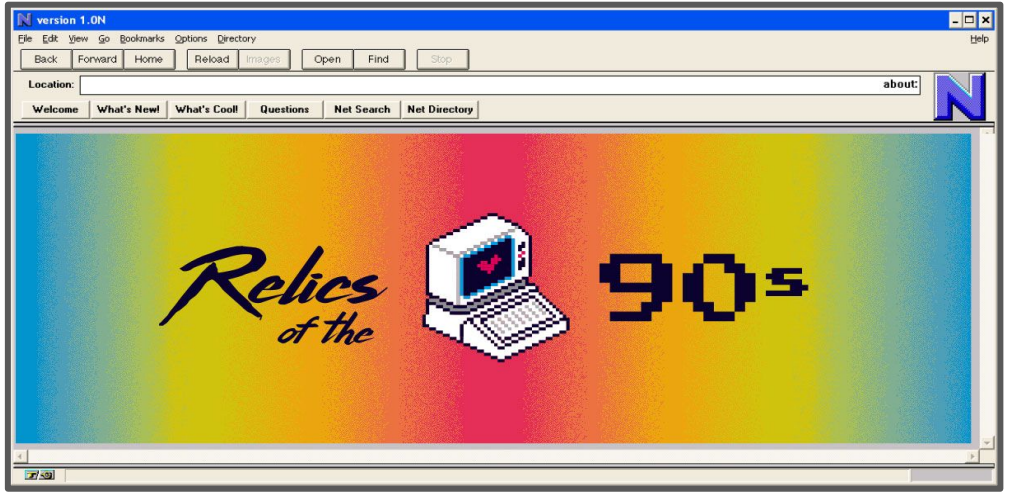
Using OpenFASOC

Mehdi Saligane
University of Michigan
mehdi@umich.edu

7th July, 2023

Evolution of Software Dev

- Software Dev in the 90s
  - Vendor provided compiler
  - Toolchain incompatibilities
  - OS dependent



Context and Background

- Software Dev in the 90s
  - Vendor provided compiler
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Looks like current hardware dev!

Lowering Costs & Barriers to Chip Design

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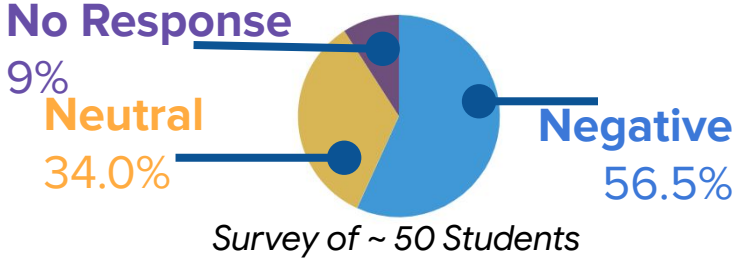
Describe your experience with (tapeout) toolchain in one word



Survey of ~ 50 Students

Lowering Costs & Barriers to Chip Design

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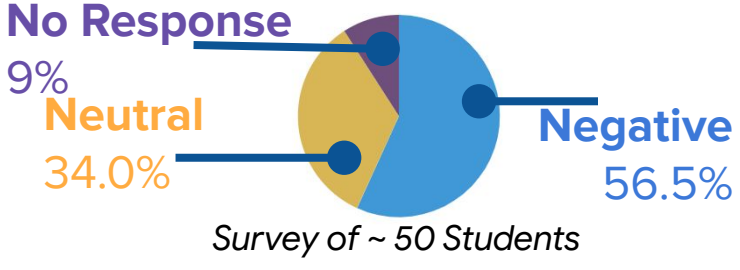

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70 000 HW vs 830 000 SW Eng.

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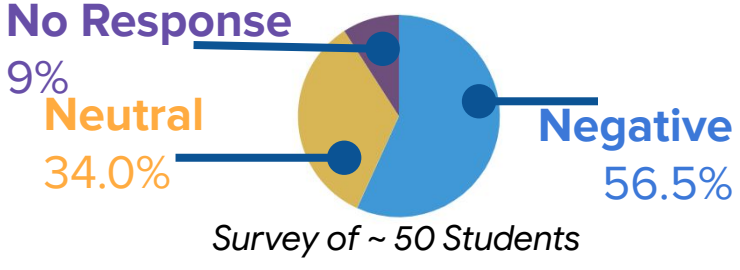

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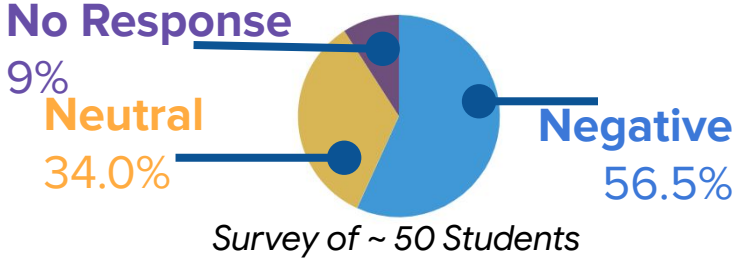

Survey of ~ 50 Students

UG student Ali Hammoud to present his winning Code-a-Chip design at ISSCC 2023

Catharine June • February 16, 2023

ECE ELECTRICAL & COMPUTER ENGINEERING UNIVERSITY OF MICHIGAN

Hammoud's project is based on the open-source hardware design tool called OpenFASoC, developed at Michigan.

Ali Hammoud, a second-year student in computer engineering, is a winner in the inaugural international Code-a-Chip competition. He will present his project in open-source chip design at the 2023 International Solid-State Circuits Conference (ISSCC), along with 6 other design teams from around the world. His design is called OpenFASoC: Digital LDO Generator.

Hammoud's design is based on the open-source tool called OpenFASoC, short for Open-Source Fully Autonomous System-on-Chip, which was co-developed by his faculty advisor on the project, Dr. Mehdi Saligane. OpenFASoC was developed for analog circuit design, which is more difficult to automate than digital circuit design.

Lowering Costs & Barriers to Chip Design

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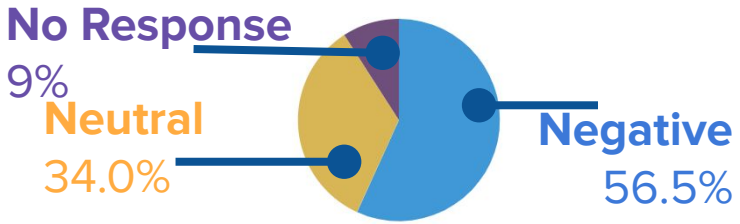

Survey of ~ 50 Students

Hardware		Software	
New deploy 18 months		Push once a week	
New Deploy	18 months	Normal Push	4-6 hours
All Replaced	~6 years	Emergency Push	<1 hours
~4 versions deployed		~1 version deployed	

70 000 HW vs 830 000 SW Eng.

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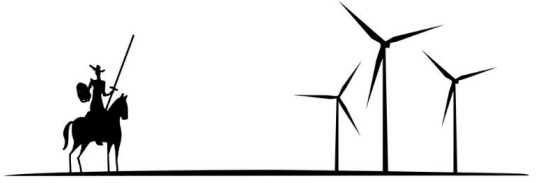

Is Hardware Development Broken?

Describe your experience with (tapeout) toolchain in one word

Survey of ~ 50 Students

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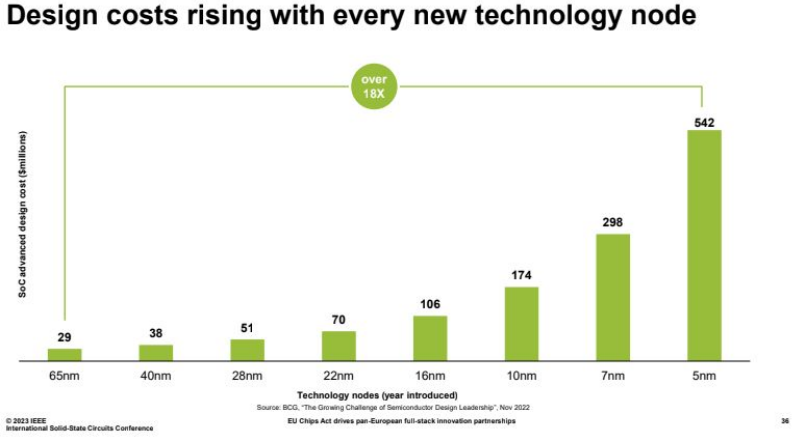
Lowering Costs & Barriers to Chip Design

- Is Hardware Development Broken?



Source: ISSCC'23 - Plenary

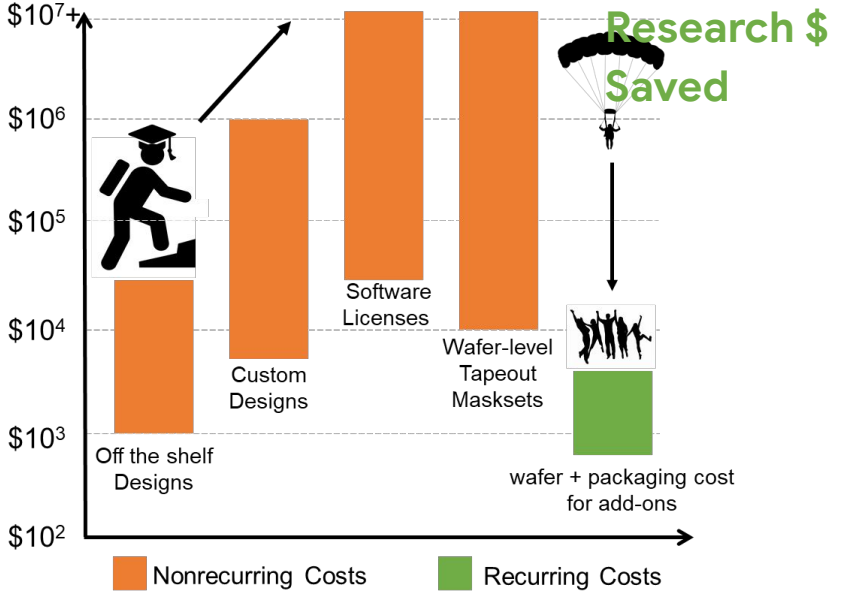
The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts

Invited Paper

Tim Ansell
tansell@google.com
Google
Mountain View, California

Mehdi Saligane
mehdi@umich.edu
University of Michigan
Ann Arbor, Michigan

- *T. Ansell and M. Saligane, "The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts : Invited Paper," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020.*



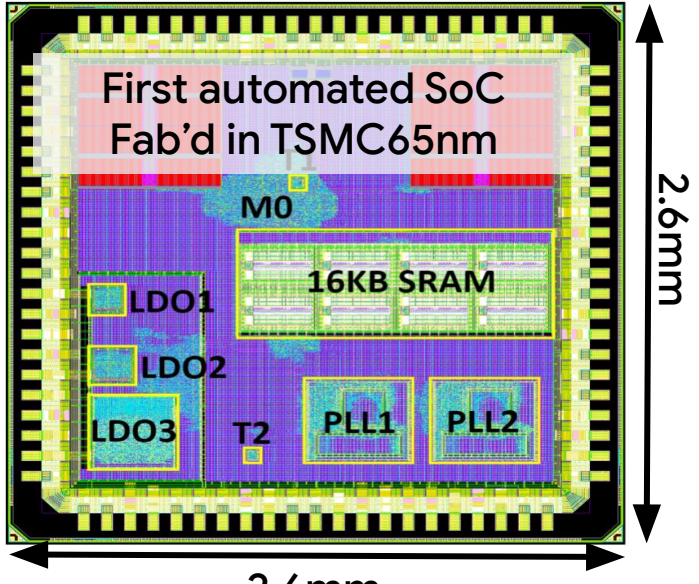
Source: NIST

Overview of FASOC

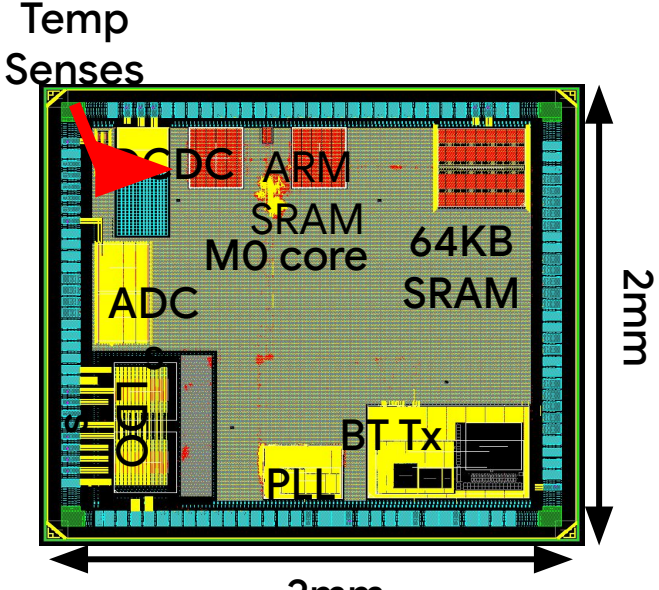
Fully Autonomous SoC Synthesis

- DARPA IDEA Program (OpenROAD and FASoC)
- Multi-University and Industry effort
- Multiple tape-outs in TSMC 65, GF12LP, SkyWater 130nm

https://fasoc.engin.umich.edu/

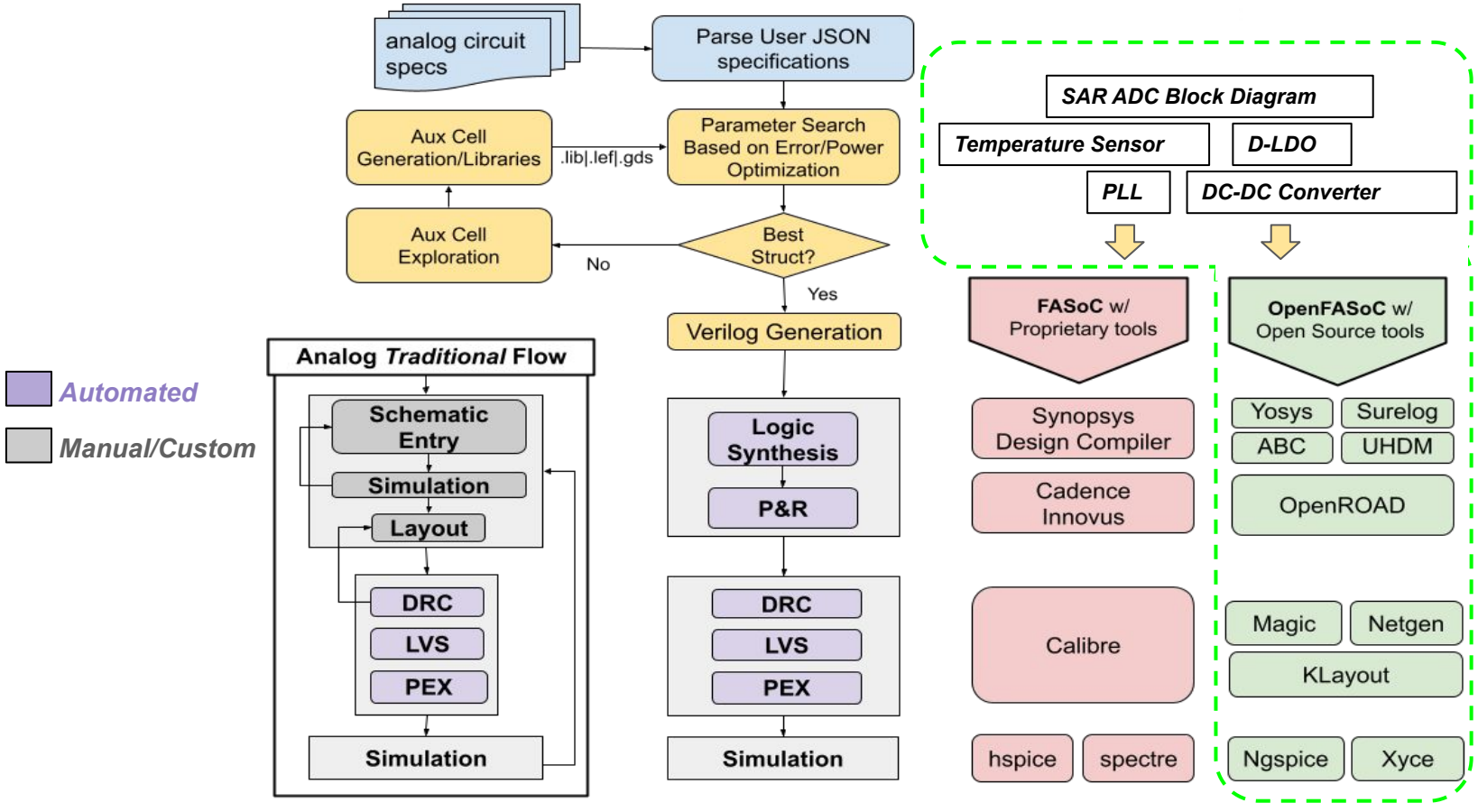


TSMC65LP SoC (2019-08)



GF12LP SoC (2020-10)

Now proprietary *or* open source design flow



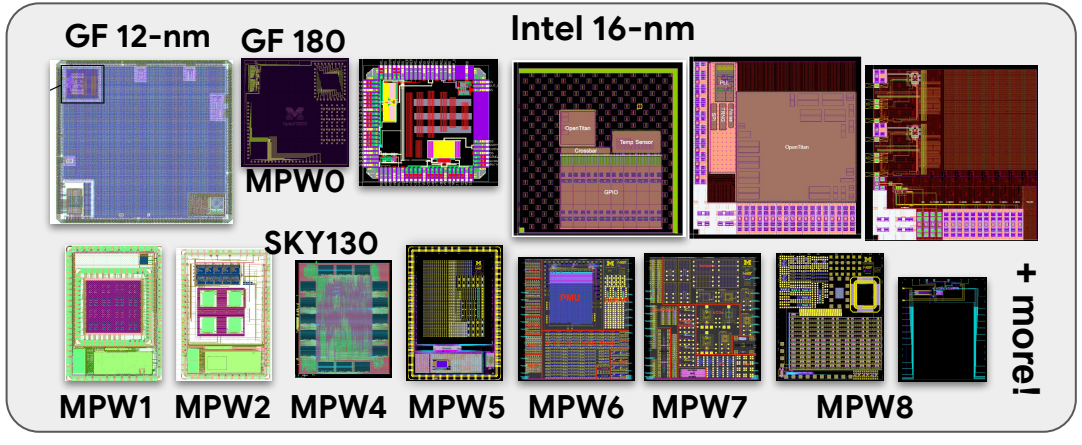
OpenFASoC!

Automated **portable** analog

Overview of OpenFASOC

Fully Autonomous SoC Synthesis

- DARPA IDEA Program, now funded by Google, NIST and others
- Multiple tape-outs in TSMC 65, GF12LP, SKY130, GF180MCU, Intel 16



<3 years, <10 people!

openfasoc.readthedocs.io

CHIPS Alliance Workshop 2021-11

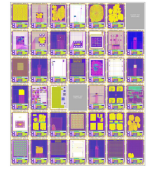
OpenPOWER AI Workshop IBM - 2022-11

CHIPS Alliance Technology Update 2022-12

RISCV Alliance Japan 2022-12

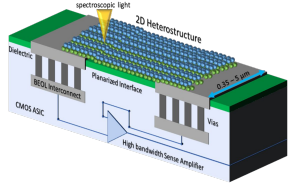
On-Going Projects & Contributions

Open-Source IC & tapeouts



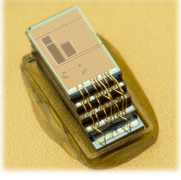
- ➔ 1st *Open* Silicon Results

NIST Nanofabrication Accelerator



- ➔ 1st *Open* Nanotechnology Platform
- ➔ Cryogenic CMOS

Low-Power IC Design



- ➔ ***Rapid*** Prototyping for Wearables

Hardware Security

- ➔ 1st *Open* Root of Trust SoC

Automated & *Open* Nanotechnology Platform

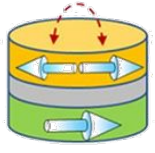
CMOS Integration Critical for Measurements

- New devices and materials are continually proposed by the academic community

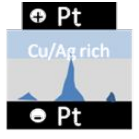
Resistive switching memory (ReRAM)

Phase Change Memory (PCM)

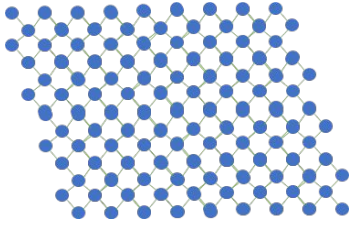
Spin Torque Transfer (STT - RAM)



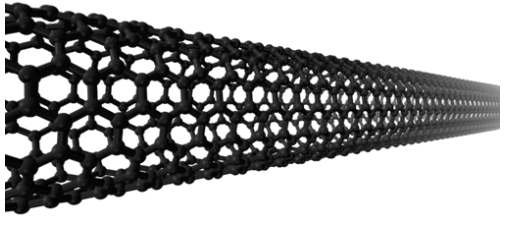
Conductive Bridge (CB-RAM)

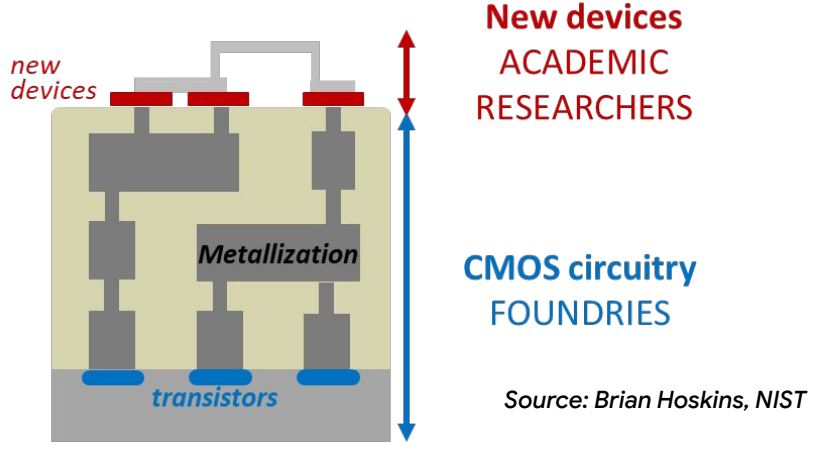


2D Materials



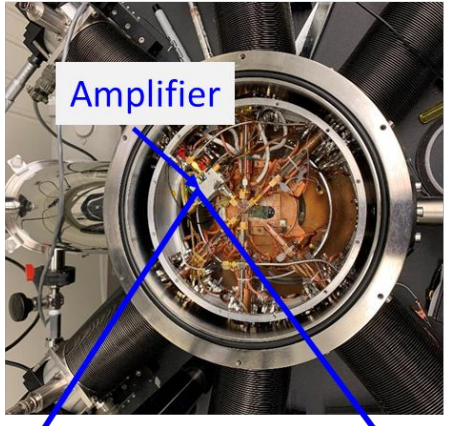
Nanotubes

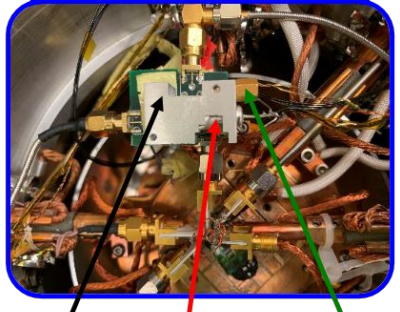




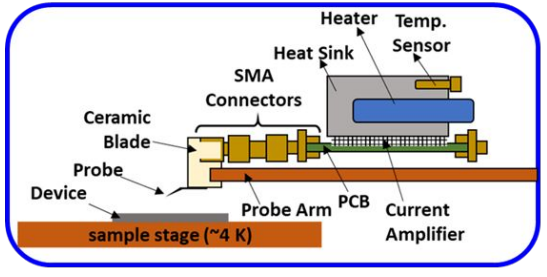
Reliable monolithic integration is a requirement for experimental prototyping

Open Cryogenic CMOS



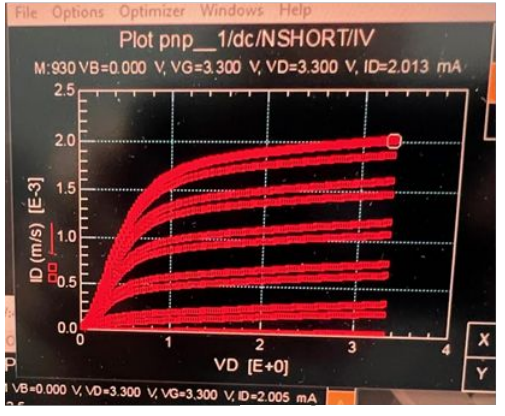


Time + Temperature dependent characterization

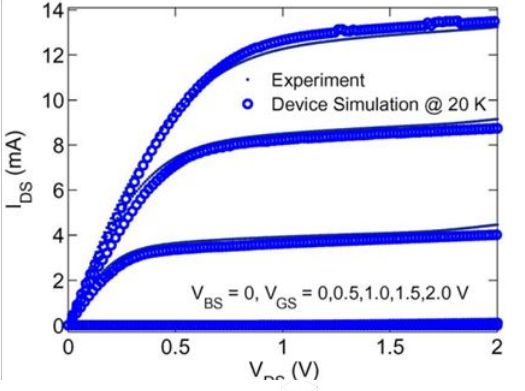


Cryogenic Models and Data of Open Sky130

Raw Data



Fit Models



Google +

NIST National Institute of Standards and Technology U.S. Department of Commerce

AIDSIR COOLCAD ELECTRONICS

skywater

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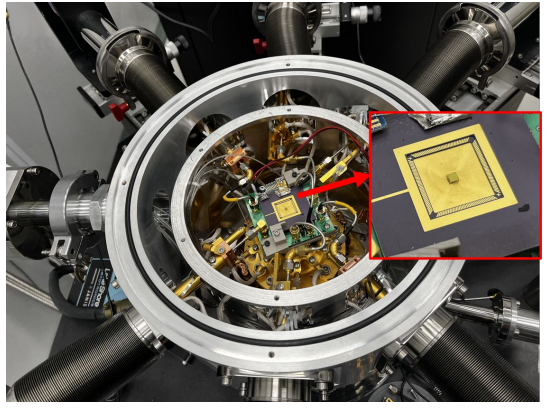
Automated PMU for Low-K Operation

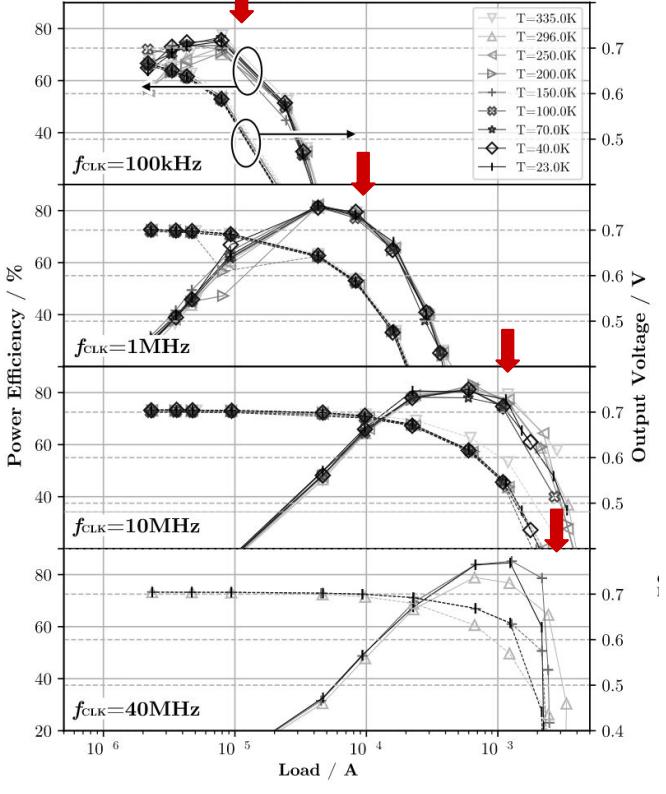
Measurement Results



Cryogenic Test Setup

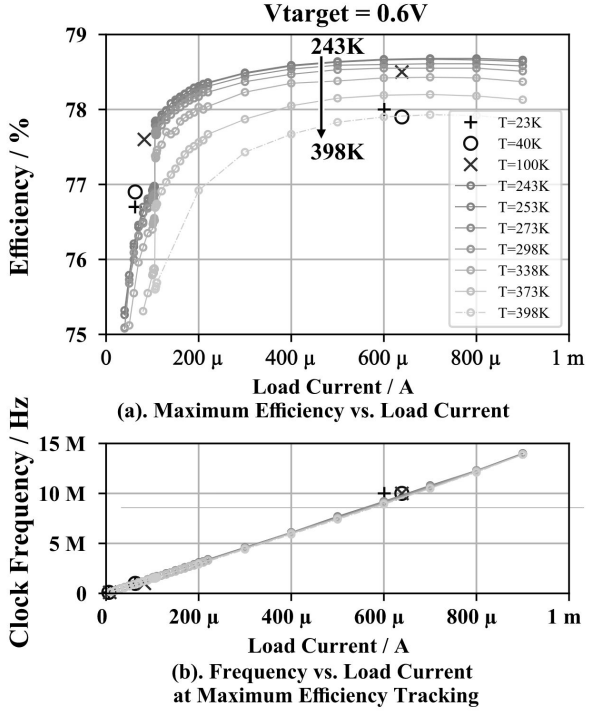
Experiments have shown constant behavior across a wide temperature range, down to cryogenic temperatures.

Maximum Eff. Point



Power Efficiency & Output Voltage
Versus Load Current, Clock Freq., and Temperature

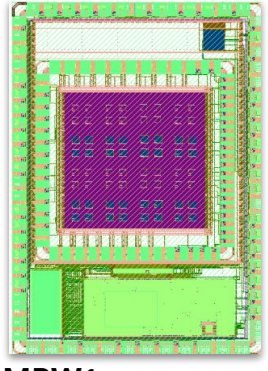
Robust against Temperature Variation



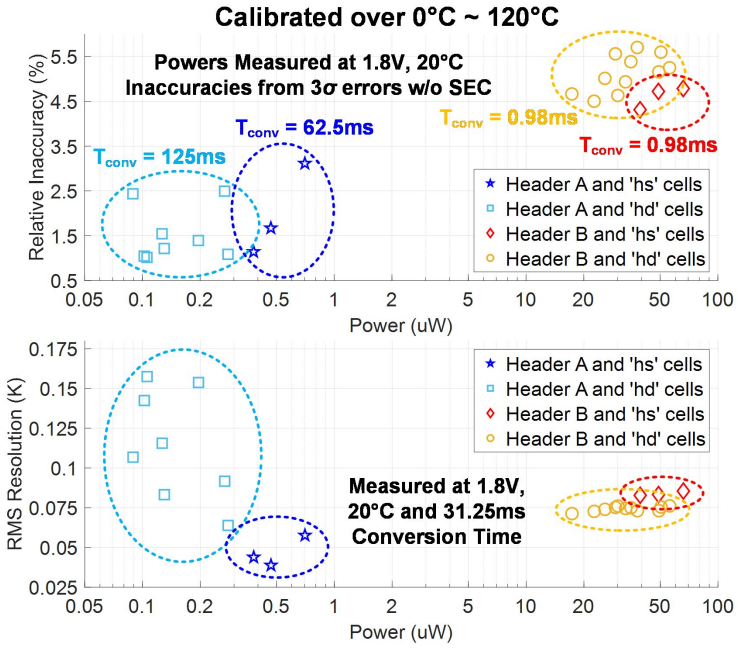
Emulated Closed-Loop Response
At Maximum-Power Tracking

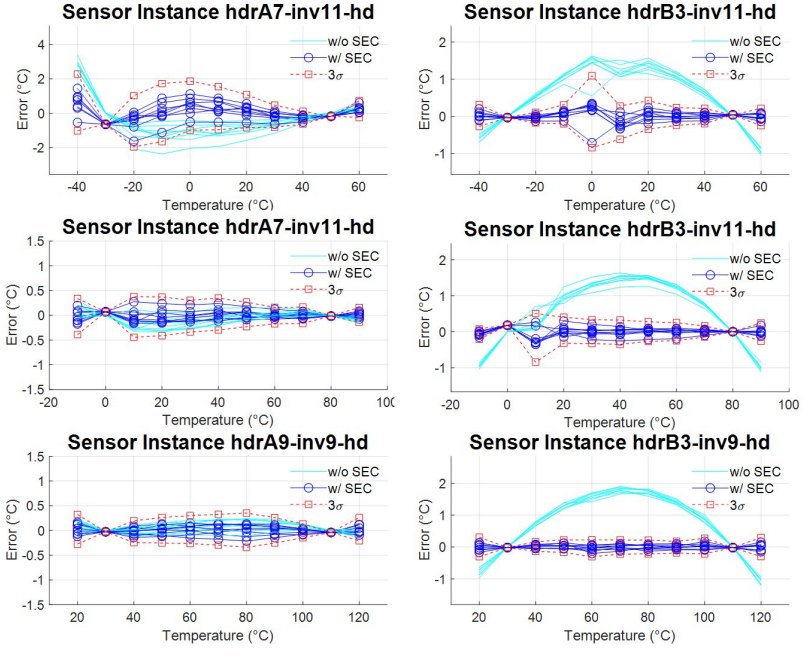
Building Confidence in *Open* Design

Start of Skywater's Open MPW Program



MPW1





Dec .... Jun Aug Oct Dec Feb Apr Jun Aug Oct Dec Feb Apr Jun

End of 2020 — 2021 — 2022 — 2024

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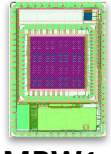
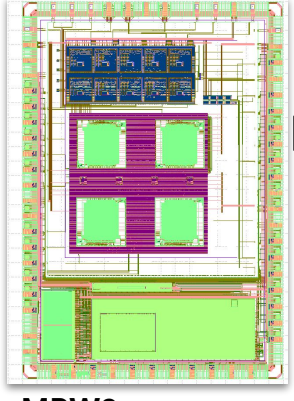
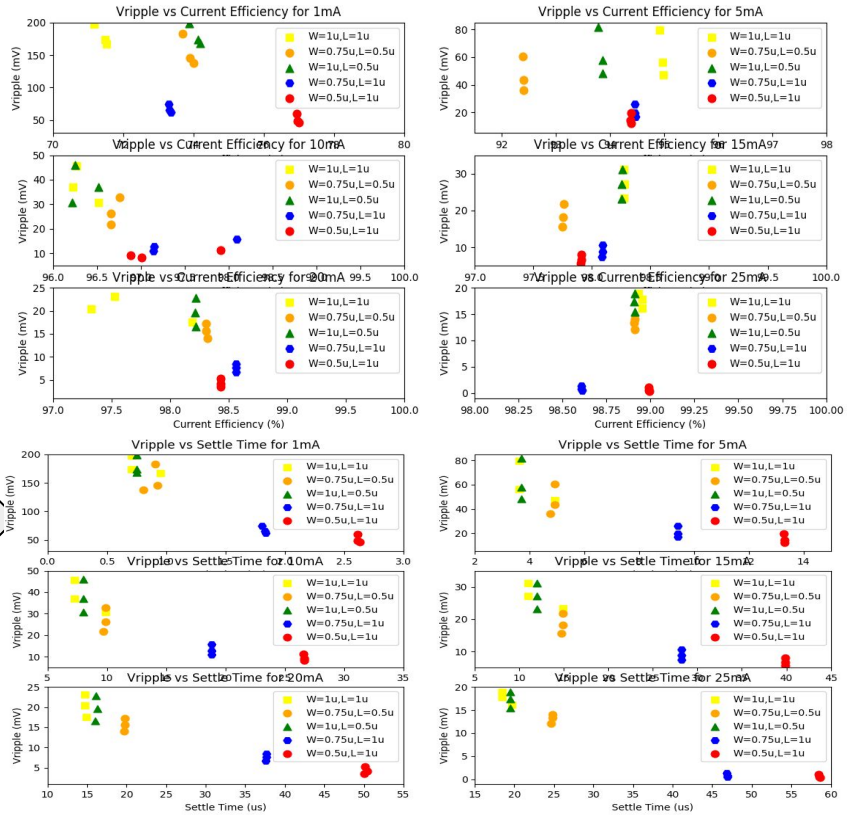
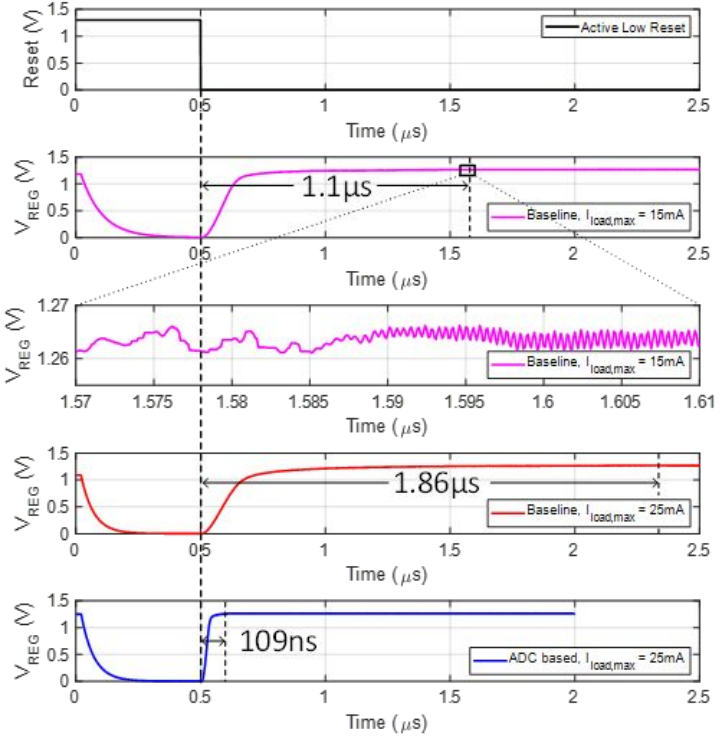


SKY130



MPW1 **MPW2**





Dec .... Jun Aug Oct Dec Feb Apr Jun Aug Oct Dec Feb Apr Jun

End of 2020 2021 2022 2024

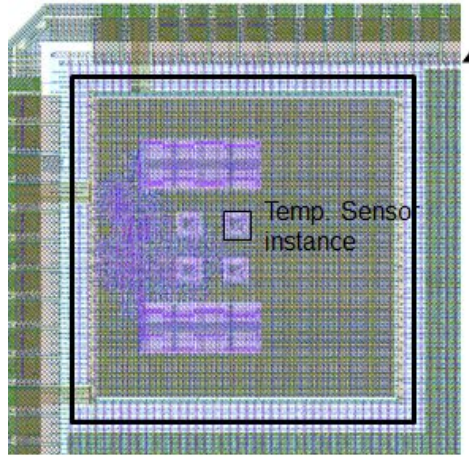
Building Confidence in *Open* Design

Tapeout throughDARPA IDEA Program

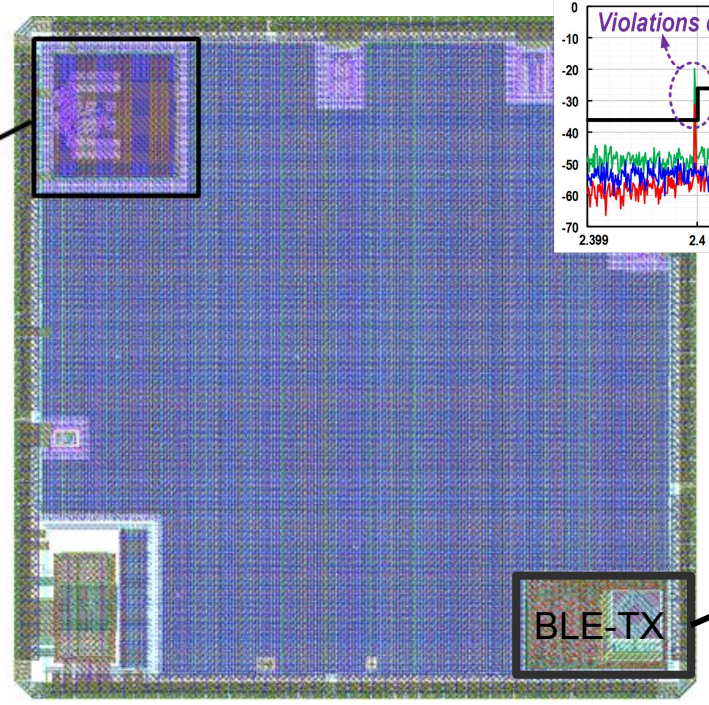
- 1st tapeout in GF12LP using open source tools

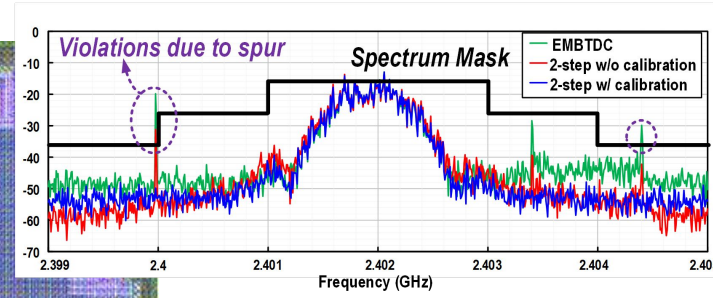
- Signoff using PT
  - @ TT|25C|0.8v|funcmax

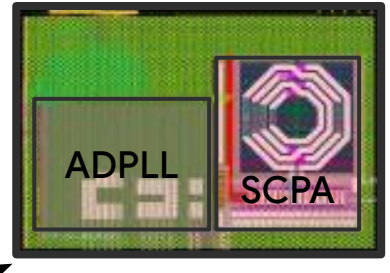
  350MHz
- Temperature sensors
  - T_{RANGE}: -20 to 100ºC
  - Error: +/- 0.2ºC (post-PEX)



GF 12-nm







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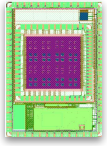
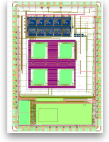




MPW1 **MPW2** MPW3

Dec .... Jun Aug Oct Dec Feb Apr Jun Aug Oct Dec Feb Apr Jun

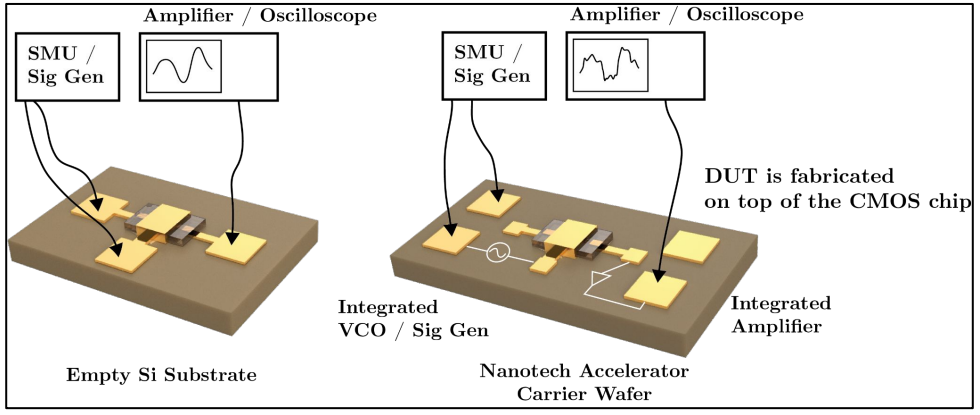
- ADPLL supports **1.8 to 2.7GHz**

End of 2020 — 2021 — 2022 — **Feb 24th** — **May 28th** — 2024

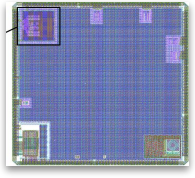
Building Confidence in *Open* Design

Start of Skywater's Open MPW Program

DARPA IDEA Program



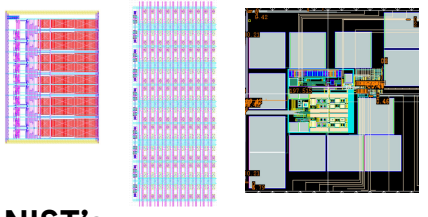
GF 12-nm



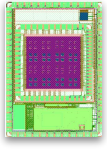
NIST

Nanofab. Accelerator program w. NIST

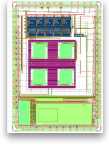
4 Testchips Already!
***Big* tapeout mid-June**



SKY130



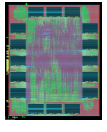
MPW1 Dec



MPW2 .... Jun

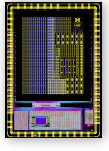
MPW3 Aug

Oct



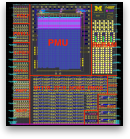
MPW4 Dec

1st TO



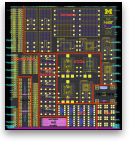
MPW5 Feb

2nd TO



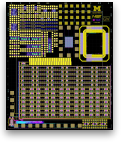
MPW6 Apr Jun

3rd TO



MPW7 Aug Oct

4th TO



MPW8 Dec Feb Apr

NIST's Nanofabrication Tapeout

Jun

End of 2020

2021

2022

Feb 24th

May 28th

2024

MICL MICHIGAN IN CIRCUITS LAI UNIVERSITY OF M

Building Confidence in *Open* Design

Start of Skywater's Open MPW Program

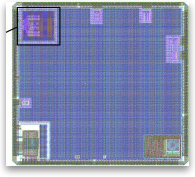
DARPA IDEA Program

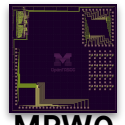
Nanofab. Accelerator program w. NIST

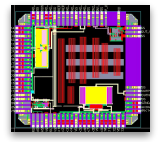
Globalfoundries Open MPW Program

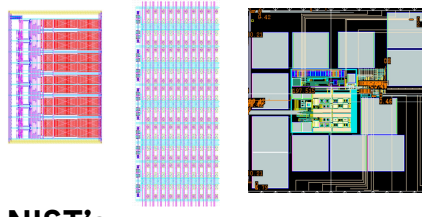
Accelerating Fitbit's Custom Silicon Goals!

fitbit

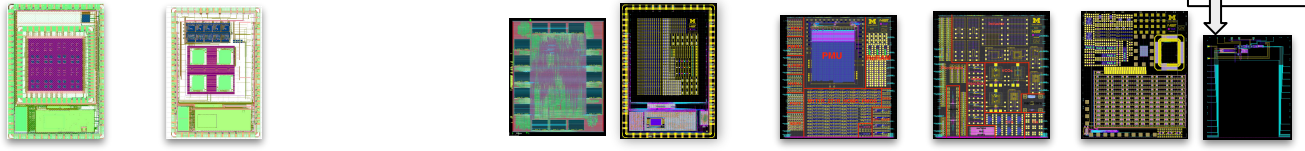








Project w. Fitbit



NIST's Nanofabrication Tapeout

MPW1 Dec .... **MPW2** Jun Aug **MPW3** Oct **MPW4** Dec **MPW5** Feb Apr **MPW6** Jun **MPW7** Aug Oct **MPW8** Dec Feb Apr Jun

End of 2020 — 2021 — 2022 — **Feb 24th** — **May 28th** — 2024

Building Confidence in *Open* Design

Intel's University Shuttle

intel foundry services

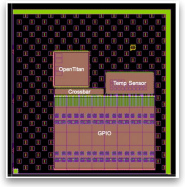
Start of Skywater's Open MPW Program

DARPA IDEA Program

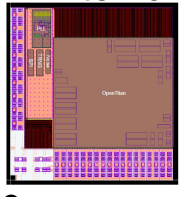
Nanofab. Accelerator program w. NIST

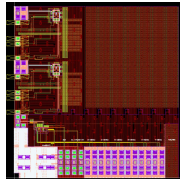
Globalfoundries Open MPW Program

Intel 16-nm

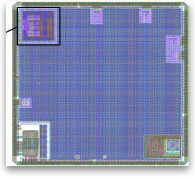


Intel 16-nm

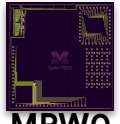




GF 12-nm

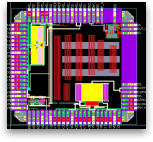


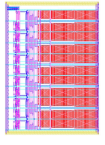
GF 180

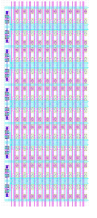


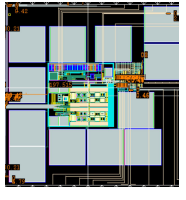
MPW0

GF 180

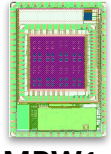


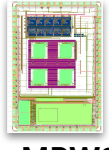


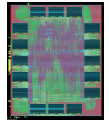


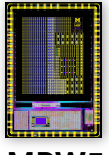


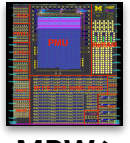
SKY130

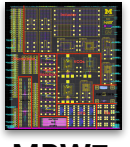


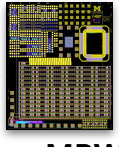


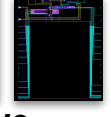












Project w. Fitbit

NIST's Nanofabrication Tapeout

MPW1	MPW2	MPW3	MPW4	1st TO MPW5	2nd TO MPW6	3rd TO MPW7	4th TO MPW8				
Dec	.... Jun	Aug	Oct	Dec	Feb	Apr	Jun	Aug	Oct	Dec	Feb	Apr	Jun

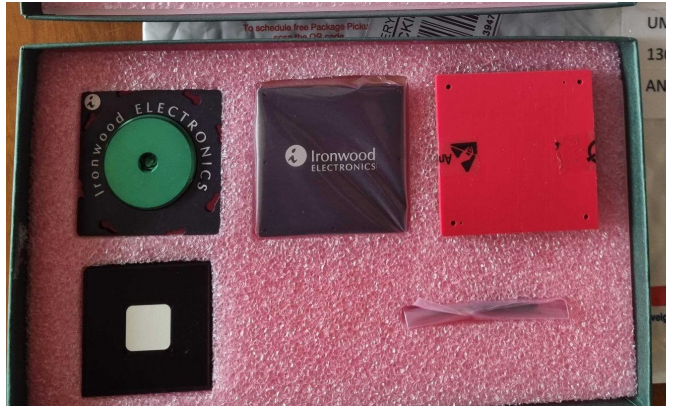
End of 2020 — 2021 — 2022 — Feb 24th — May 28th — 2024

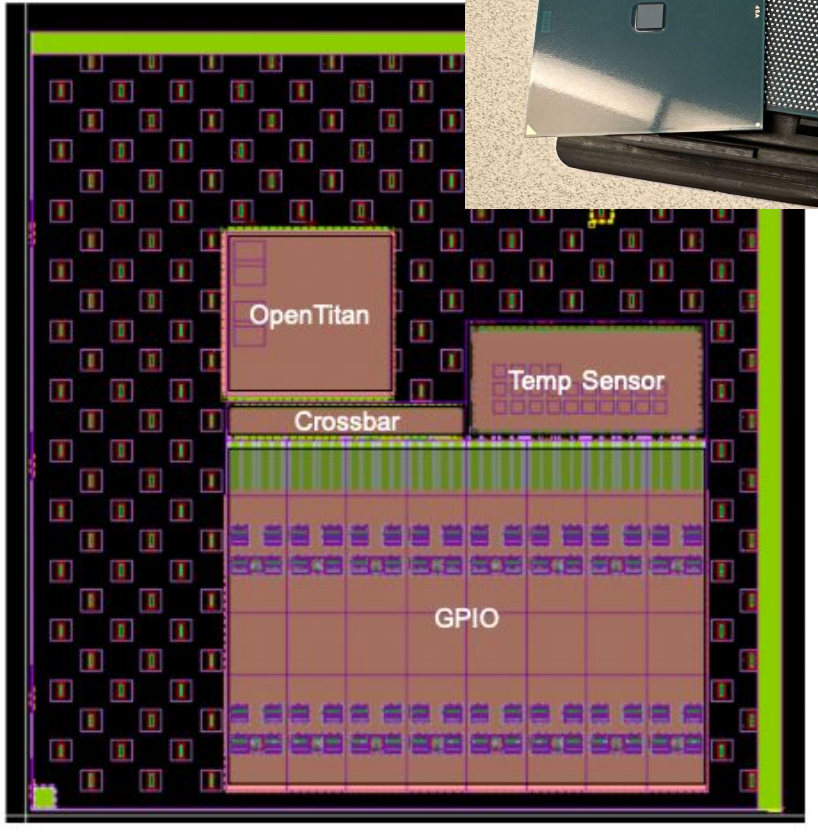
We *Need* More Shuttles!

Tape Outs in Intel 16 - OpenTitan SoC

- Tapeout in Intel 16nm using OS tools
- PD and timing optimization using OpenROAD
- Used a modular flow to smoothly fill-in the gaps using proprietary tools

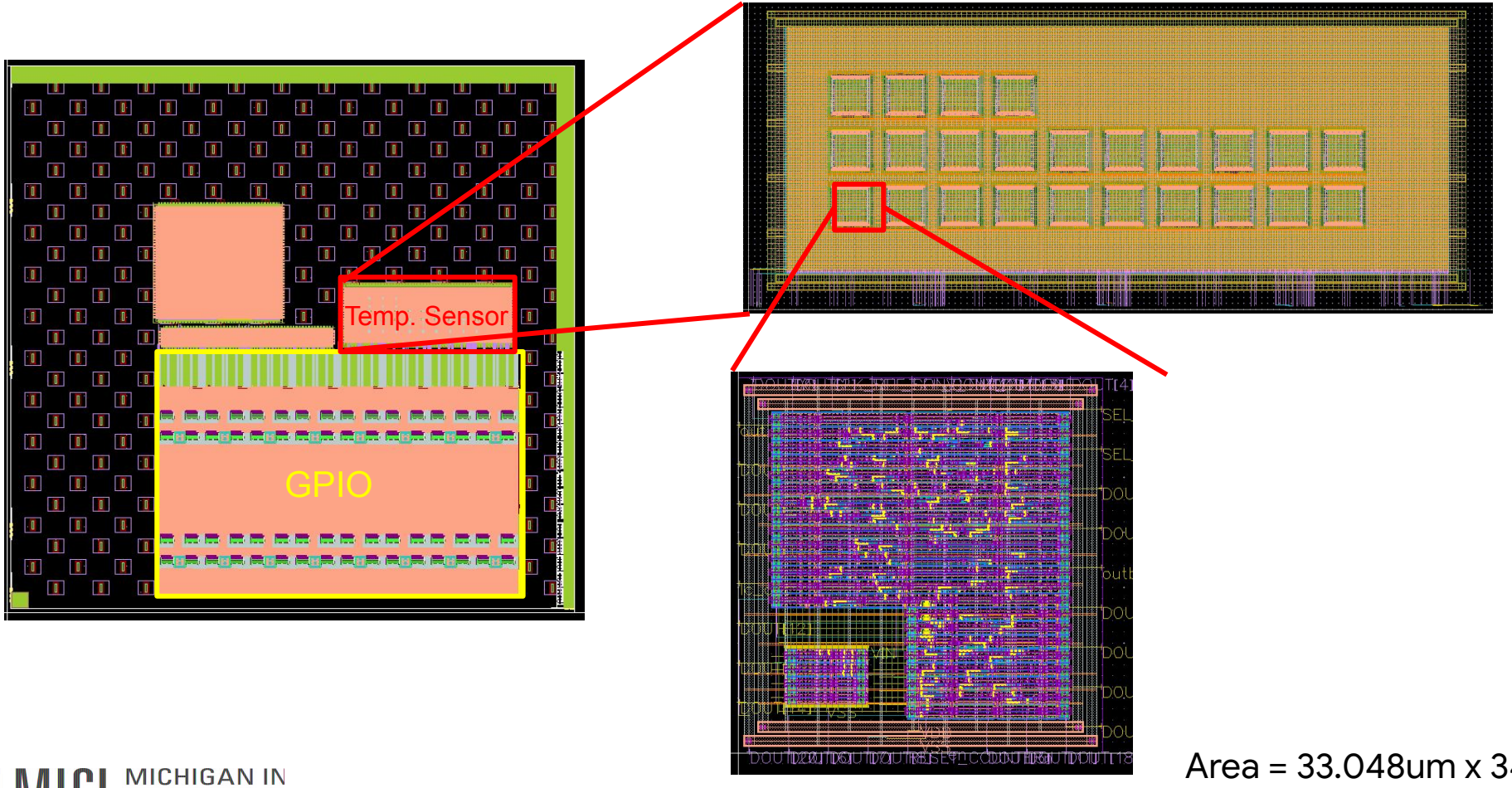
- Temperature Sensor RTL to GDS flow is fully Open-Source





Floorplan of Intel 16 tapeout Including Opentitan, Temperature sensor array and crossbar using OpenROAD

24 Temperature Sensors Array

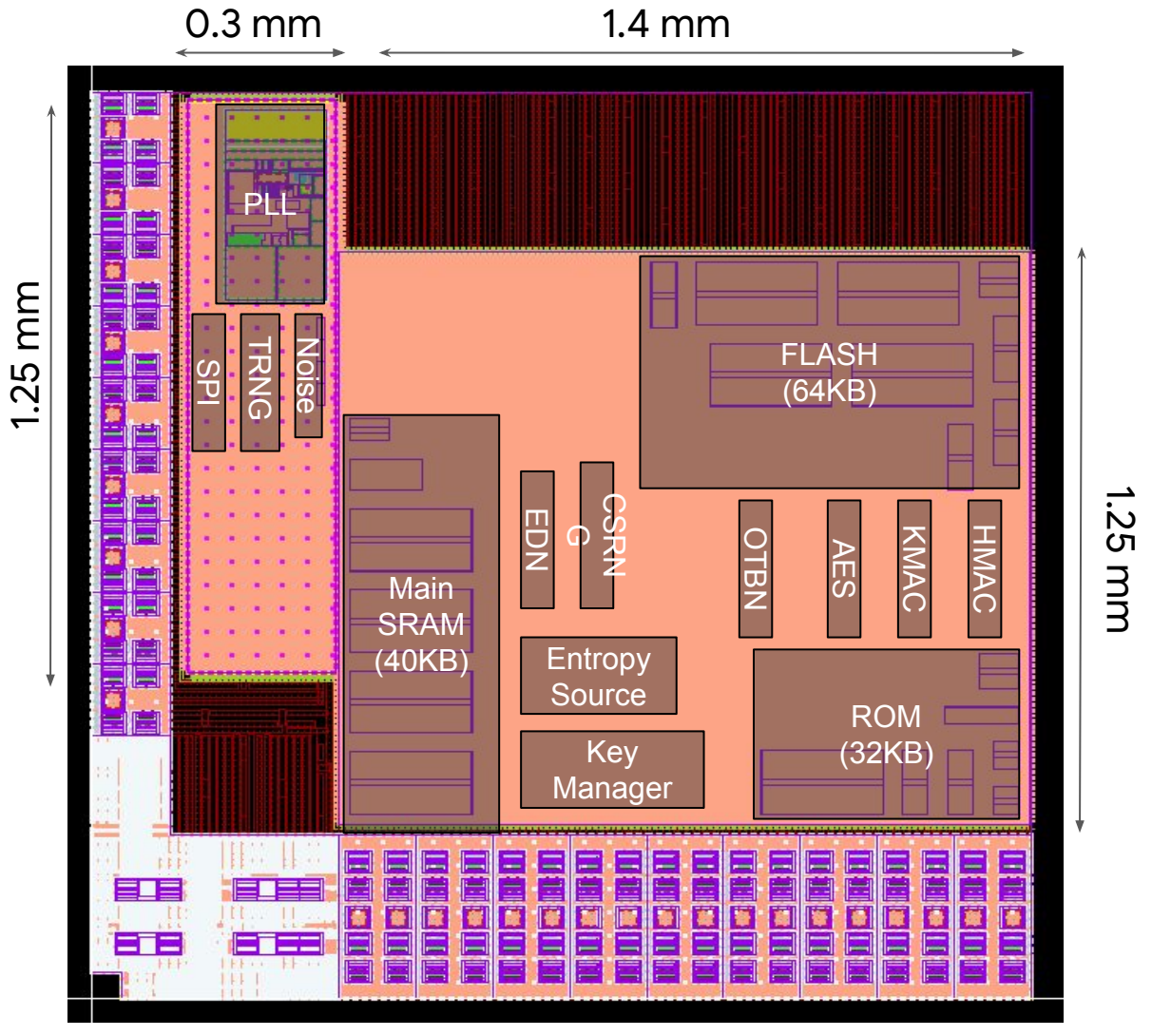


Area = 33.048um x 34.02um

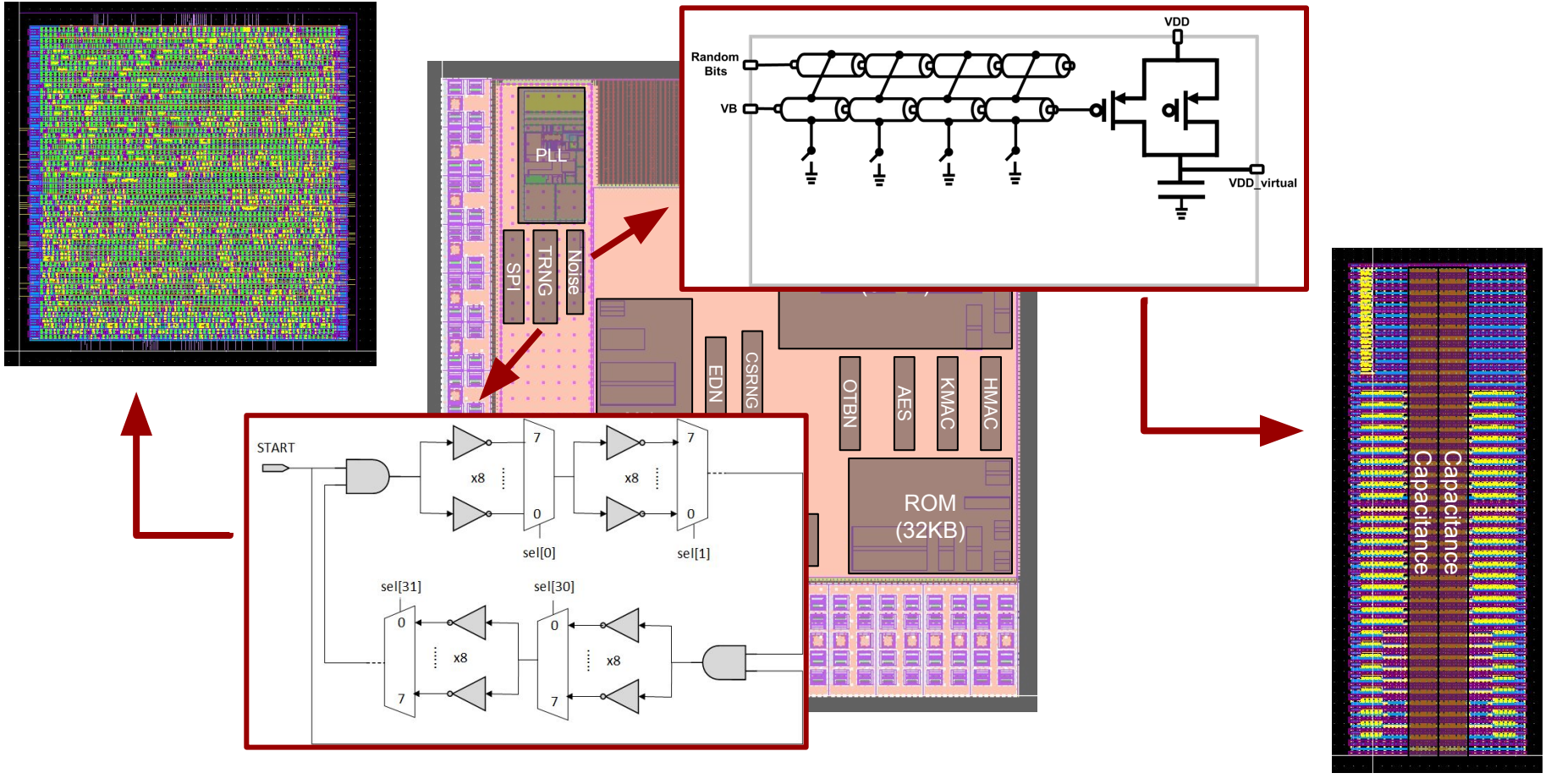
OpenTitan Root of Trust SoC - Final Version

- All digital edge tracing TRNG
- Tunable Noise Injection
- On-chip high speed PLL
- OpenTitan security subsystem
  - Crypto + Key Manager
  - Secure Memory

Frequency	28MHz
Memory Size	16KB
Gate Count	20K
# of Macros	26
Area	2.18mm^2



OpenTitan Root of Trust SoC - Final Version



What is next?

Bridging Gaps between Hardware & Software

Make custom silicon easier to build, at scale, just like software

```
$ gcc -OSilicon
```

"My god,
it's full of software!"

Bridging Gaps between Hardware & Software

Packaging
conda-eda
github.com/hdl/conda-eda

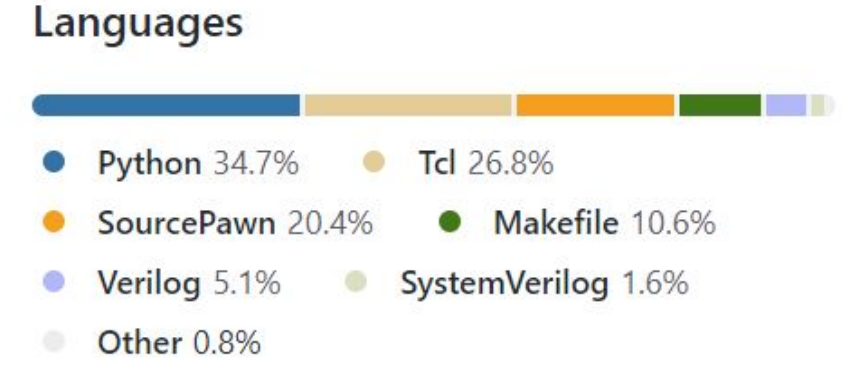
```
conda install --channel litex-hub \
              open_pdks.sky130a   \
              openlane            \
              xls
```

"My god,
it's full of software!"

Reproducible, Reusable
Jupyter Notebook
github.com/chipsalliance/silicon-notebooks/

Bridging Gaps between Hardware & Software

- OpenFASOC GitHub Repo is mainly Code and Documentation



"My god,
it's full of software!"

Bridging Gaps between Hardware & Software

- OpenFASOC GitHub Repo is mainly Code and Documentation
  - Auditable and Transparent
  - Regression Tests
  - Systematic Metrics Extraction
  - Dashboards

"My god,
it's full of software!"

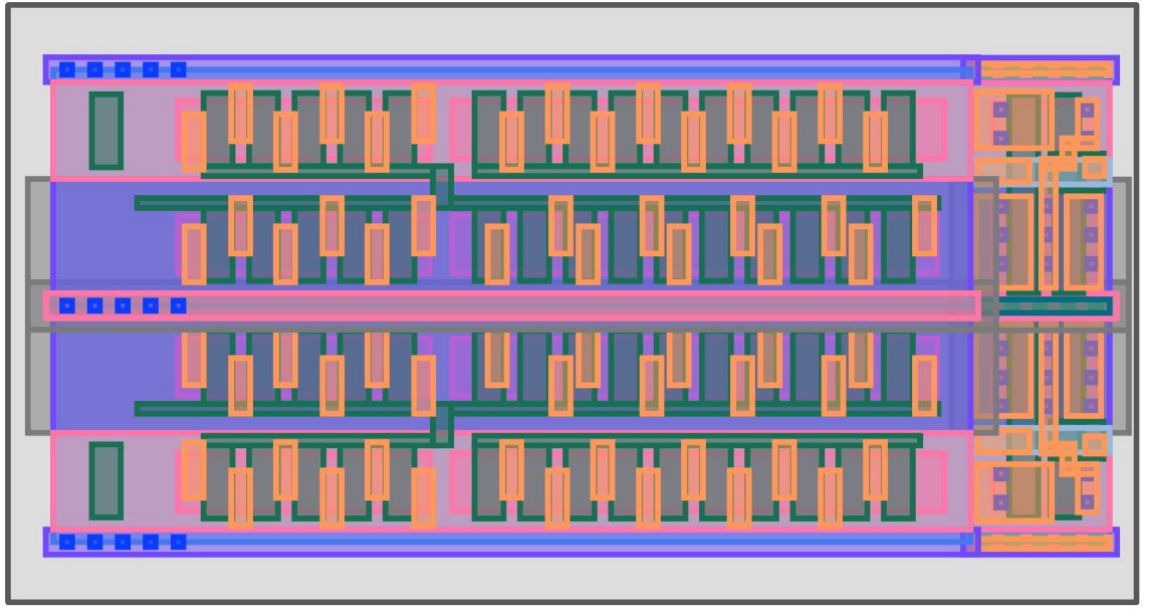
Bridging Gaps between Hardware & Software

- OpenFASOC GitHub Repo is mainly Code and Documentation
  - Auditable and Transparent
  - Regression Tests
  - Systematic Metrics Extraction
  - Dashboards
- Analog Automation requires collaborative Work
  - EDA, Analog/RF/Circuits, Software

"My god,
it's full of software!"

Generator with a Higher Control/Precision

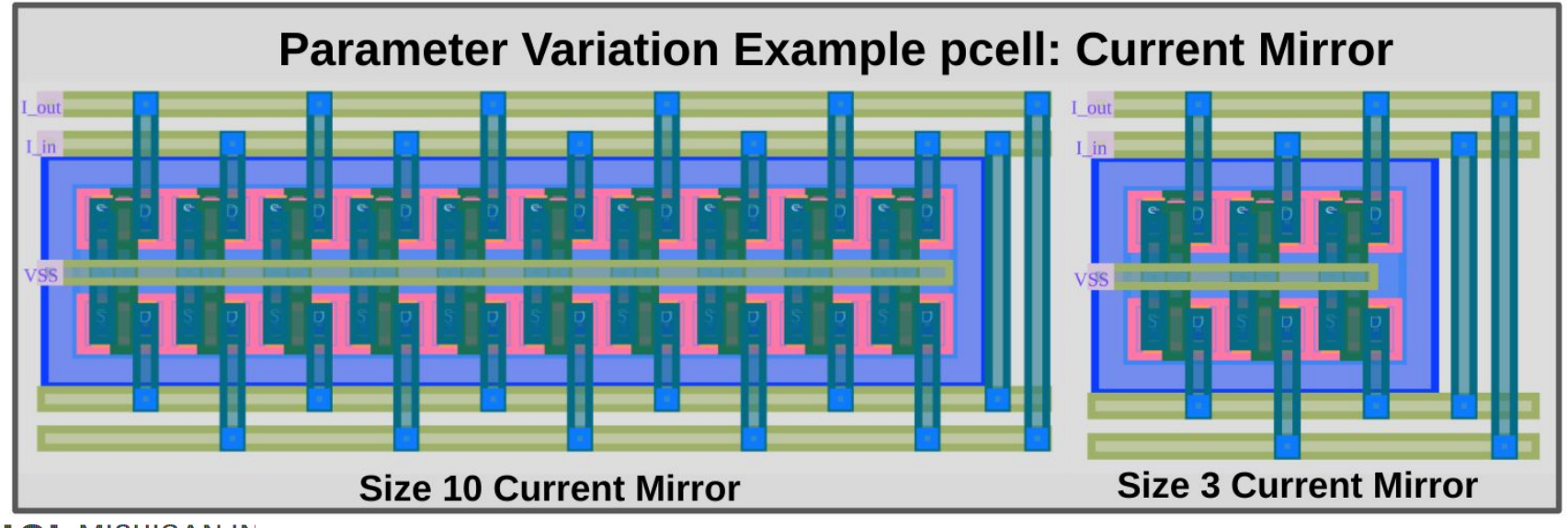
- Addresses porting Aux-cells to new PDK
- Programmatic layout provide fine control with automation



Auto-Generated Comparator Cell

Generator with a Higher Control/Precision

- Object oriented code provides flexibility
- PDK -> py class
- Generators -> py function
- User codes hardware by importing py packages



Integration with GDSfactory & OpenROAD

OpenFASOC with GDSFactory Generator API

Python PDK

Technology Layers
PDK.get_layer()

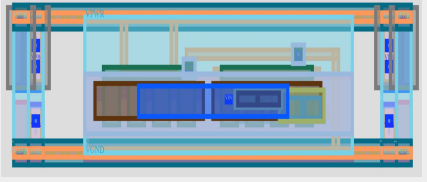
DRC Rule Deck

Component Lib
PDK.get_component()

Generator

```
# function interface
@gf.cell
def top(args, PDK):
        …
        return top
```

e.g Voltage Header Cell



Imports

User Created PY Script

```
import [PDK]
import openfasoc.[Generator]

cell = [Generator].top(args,PDK)
cell.write_gds()
```

Integrating Cells

1. **Defined cell placement**
2. **Auto route**

Reproducible, *Reusable* **Results** using Notebooks & *Open* PDKs

- **Selected** by the US Consulate in Japan to organize **workshops** and **training** for the Japanese **Workforce** in Kyushu Area

U.S. EMBASSY & CONSULATES IN JAPAN

U.S. DEPARTMENT OF STATE

U.S. Consulate Fukuoka

Notice of Funding Opportunity

Funding Opportunity Title:	FY2023 U.S. Consulate Fukuoka: High-Tech Labor Force Curriculum Development Workshop
Funding Opportunity Number:	FUKUOKA-PAS-FY23-02
Deadline for Applications:	February 19, 2023 (by 11:59 pm JST)
Assistance Listing Number:	19.040 – Public Diplomacy Programs

Reproducible, *Reusable* **Results** using Notebooks & *Open* PDKs

- **Selected** by the US Consulate in Japan to organize **workshops** and **training** for the Japanese **Workforce** in Kyushu Area
  - Partnering with local Universities

U.S. EMBASSY & CONSULATES IN JAPAN

U.S. DEPARTMENT OF STATE

U.S. Consulate Fukuoka

Notice of Funding Opportunity

…3 U.S. Consulate Fukuoka: High-Tech Labor Force
…ulum Development Workshop
…OKA-PAS-FY23-02
…y 19, 2023 (by 11:59 pm JST)
… Public Diplomacy Programs

Tokyo, PASGrants <TokyoPASGrants@state.gov> May 1, 2023, 3:05AM
to Strader, Masayuki, Tracy, Caitlin, me, Michelle

Dear Tracy Schwab,

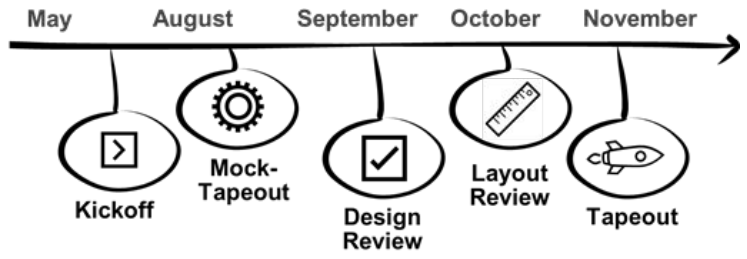
Your application submitted on February 18, 2023 in response to the U.S. Consulate Fukuoka's Notice of Funding Opportunity FUKUOKA-PAS-FY23-02, has been selected for funding.

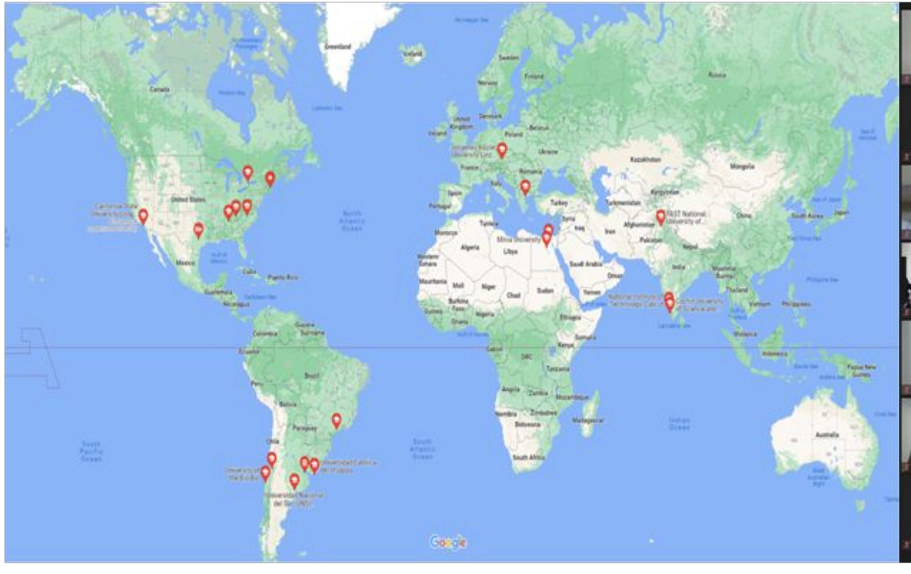
The Grants Officer and the Grants Officer Representative for your proposed project are as follows:
Grants Officer: Strader Payton
Grants Officer Representative: Masayuki Miyauchi

IEEE SSCS TC OSE Activities

SSCS PICO Chipathon

- 2021: 61 submissions, 18 selected (11 taped out)
- 2022: 54 submissions, 22 selected (14 taped out)



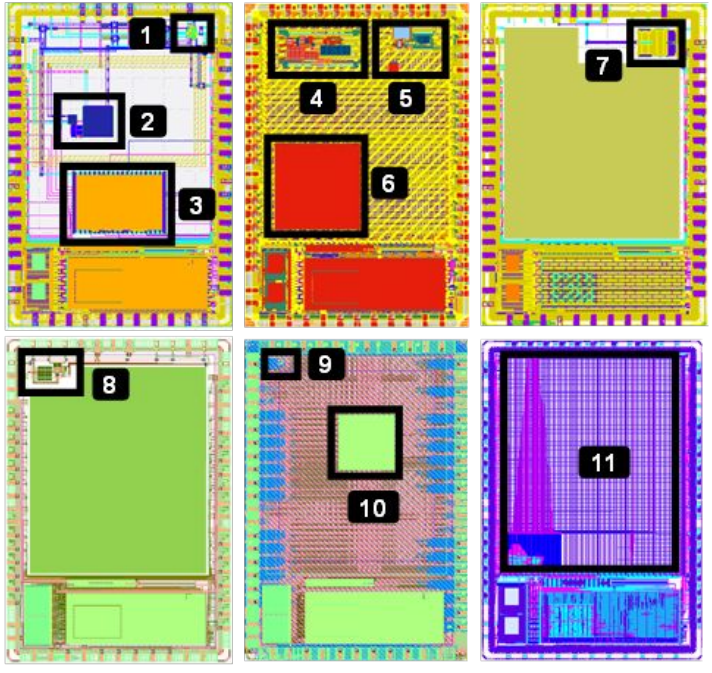


2022 selected teams from 10 countries, 5 continents

June 22, 2022, kick-off meetup with over 100 attendees

gram

2021 Chipathon

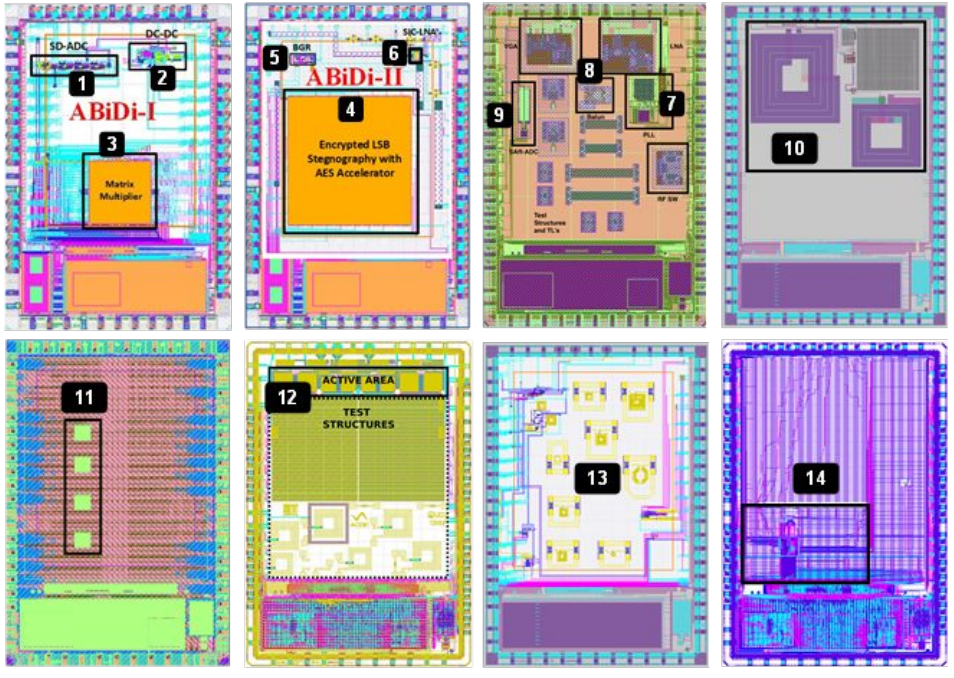


	Function	Team	Chip URL
1	5G bidirectional amplifier	Pakistan3 (FAST National University)	https://efabless.com/projects/560
2	Wireless power transfer unit	Pakistan2 (FAST National University)	
3	Variable precision fused multiply-add unit	Pakistan1 (FAST National University)	
4	Oscillator-based LVDT readout	India2 (Anna University)	https://efabless.com/projects/474
5	Temperature sensor	India1 (Anna University)	
6	GPS baseband engine	India3 (Anna University)	
7	Ultra-low-power analog front-end for bio signals	Brazil2 (U. Federal de Santa Catarina)	https://efabless.com/projects/476
8	TIA for quantum photonics interface	USA4 (University of Virginia)	https://efabless.com/projects/470
9	Bandgap reference	Egypt (Cairo University)	https://efabless.com/projects/473
10	Neural network for sleep apnea detection	USA2 (University of Missouri)	
11	SONAR processing unit	Chile (University of the Bio-Bio)	https://efabless.com/projects/540

- Paid runs via Efabless chipIgnite (130 nm SkyWater)
- All designs are open source

Magazine article: "SSCS PICO Contestants Cross the Finish Line," https://ieeexplore.ieee.org/document/9694491

2022 Chipathon

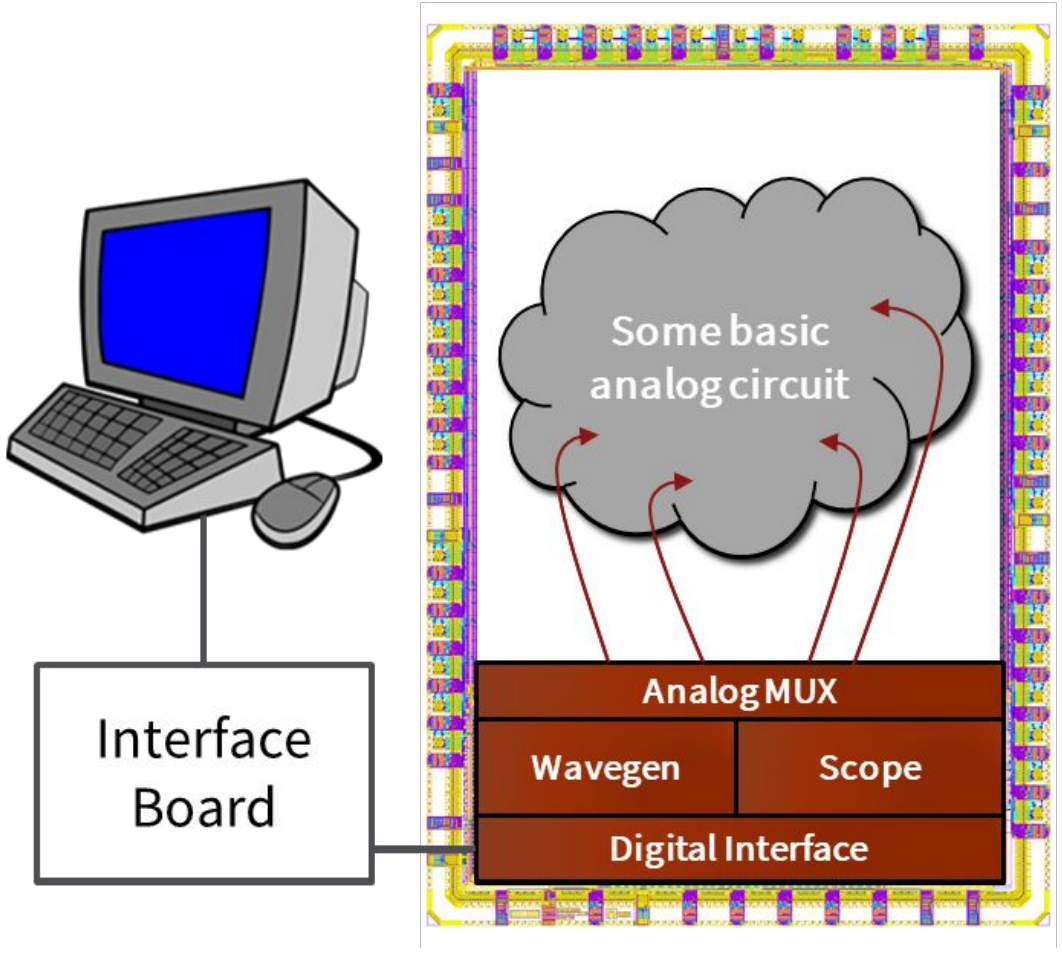


	Function	Team	Chip URL
1	Spatial Sigma-Delta ADC	Pakistan1 (FAST National University)	https://platform.efabless.com/projects/1486
2	On-Chip DCDC Converter with Fast Transient Response	Pakistan4 (FAST National University)	
3	Matrix Multiplier for AI at the Edge	Pakistan7 (FAST National University)	
4	Encrypted LSB Steganography with AES Accelerator	Pakistan2 (FAST National University)	https://platform.efabless.com/projects/1443
5	CMOS Bandgap Reference	Pakistan3 (FAST National University)	
6	Self-Interference Cancellation LNA	Pakistan4 (FAST National University)	
7	Sub-Sampling PLL for SerDes Applications	Austria (Johannes Kepler Univ., Linz)	https://platform.efabless.com/projects/1431
8	60 GHz Demonstrator Chip	Brazil (University of São Paulo)	
9	Low-Power 10-bit SAR ADC	USA1 (University of Alabama & MIT Lincoln Lab)	
10	Boost Converter for Battery-Powered IoT Applications	Greece (Aristotle University of Thessaloniki)	https://platform.efabless.com/projects/1457
11	Radiation-Hardened ALU	USA2 (North Carolina A&T State University)	https://platform.efabless.com/projects/1593
12	DC-DC Buck Converter for CubeSat	Chile[1]/Argentina[2]/Uruguay[3] [1]Universidad Técnica Fed. Santa María [2]Universidad Nacional del Sur & Instituto Nacional de Tecnología Industrial [3]Universidad Católica	https://platform.efabless.com/projects/1427
13	Electrochemical Water Quality Monitoring	USA5 (University of Tennessee)	https://platform.efabless.com/projects/1469
14	Mix-Pix - A Mixed-Signal Circuit for Smart Imaging	Chile (Universidad del Bío-Bío)	https://platform.efabless.com/projects/1494

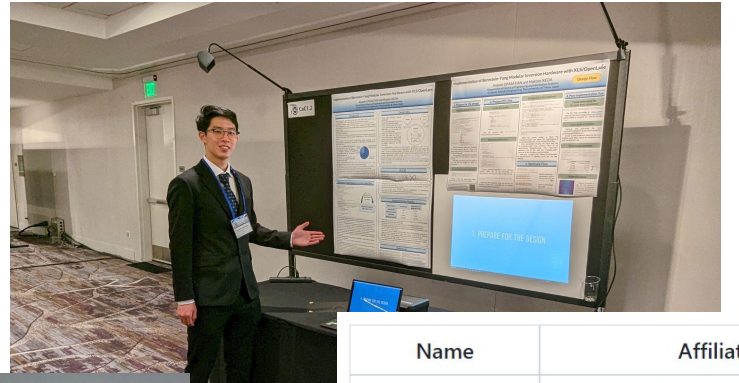
Magazine article: "Meet the SSCS PICO Chipathletes," https://ieeexplore.ieee.org/document/9950763

2023 Chipathon (Ongoing)

- Build on-chip waveform generator and “oscilloscope” macros
  - Collection of generally useful IP blocks
- Enable testing of low frequency analog circuits using only a PC
- Tape out first prototypes and improve with community over time



Notebook Code a Chip Competition at ISSCC'23



Name	Affiliation	Notebook Title
Yihai Zhang	Tsinghua-Berkeley Shenzhen Institute, Tsinghua University China	GreenRio 2: A Linux-compatible RISC-V Processor Developed with A Fully Open-Source EDA Flow
Anawin Opasatian	University of Tokyo (Japan)	Bernstein-Yang Modular Inversion with XLS/OpenLane
Mauricio Montanares	University of Concepción (Chile)	Sonar On Chip Project
Nealson Li	Georgia Institute of Technology (USA)	Coordinate Rotation Digital Computer (CORDIC) with OpenLane
HyungJoo Park	Hanyang University (South Korea)	Scan Register layout generation using laygo2
Ali Hammoud	University of Michigan (USA)	OpenFASoC: Digital LDO Generator
Nimish Shah	KU Leuven (Belgium)	DPU: DAG Processing Unit for probabilistic ML and sparse matrix algebra

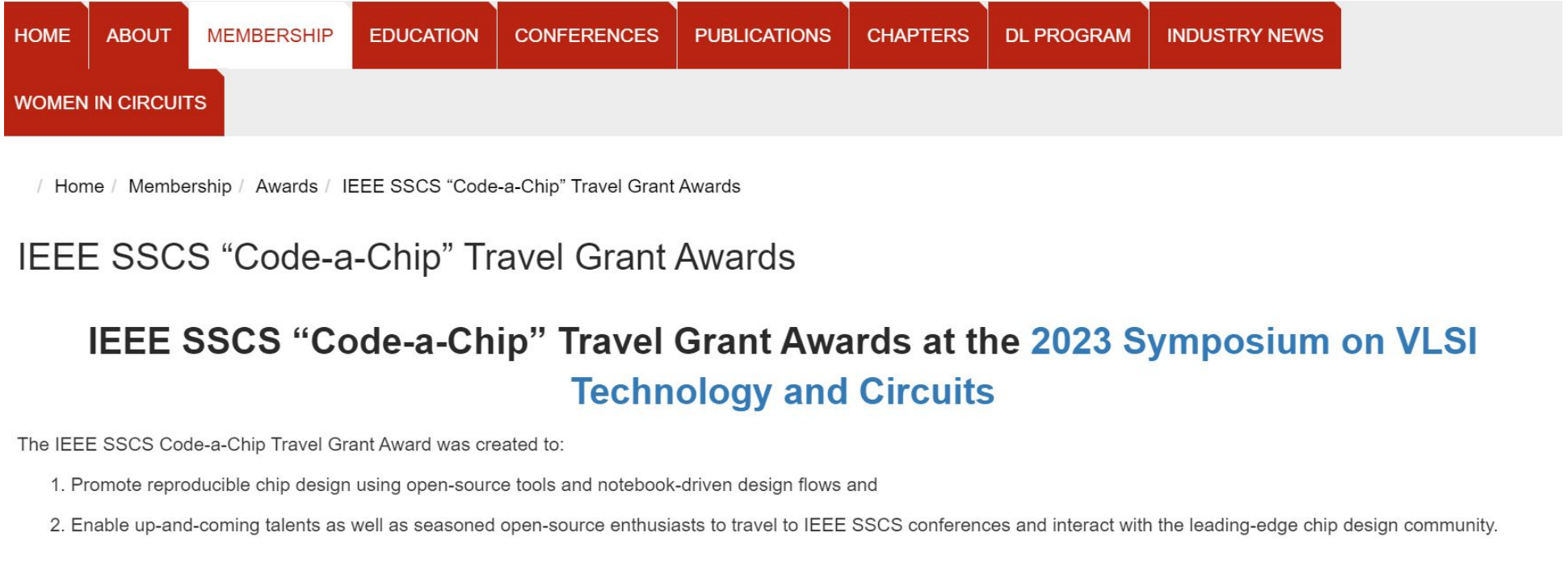
Notebook Code a Chip Competition at VLSI'23

Example: Winner of VLSI 2023 Code-a-Chip Contest

https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io/blob/main/VLSI23/accepted_notebooks/ldo_rgcn_rl/ldo_rgcn_rl.ipynb

“Code-a-Chip” Notebook Competition at VLSI'23 - Kyoto

- IEEE Solid-State Circuits Society (SSCS) Open-Source Ecosystem (OSE)
  - https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io



Monday AM Session @ ISCAS 2023

11:30 – 13:00
Review of the First Silicon Results in the Open Source Ecosystem
Room: San Carlos III (Marriott)
Session Chair(s): Mehdi Saligane, *University of Michigan*
Priyanka Raina, *Stanford University*

11:30
2273: An Open Source Compatible Framework to Fully Autonomous Digital LDO Generation
Yaswanth Kumar Cherivirala, Mehdi Saligane, David Wentzloff
University of Michigan, Ann Arbor, United States

11:48
2290: Design of Cryo-CMOS Analog Circuits Using the Gm/ID Approach
Christian Enz, Hung-Chi Han
École Polytechnique Fédérale de Lausanne, Switzerland

12:06
2314: SRAM Design with OpenRAM in SkyWater 130nm
Jesse Cirimelli-Low{2}, Muhammed Hadir Khan{2}, Samuel Crow{2}, Amogh Lonkar{2}, Bugra Onal{2}, Andrew Zonenberg{1}, Matthew Guthaus{2}
{1}IO Active, United States; {2}University of California, Santa Cruz, United States

11:24
2326: An Open-Source 4x8 Coarse-Grained Reconfigurable Array Using SkyWater 130 nm Technology and Agile Hardware Design Flow
Po-Han Chen, Charles Tsao, Priyanka Raina
Stanford University, United States

12:42
2327: Open-Source, End-to-End Auditable Tapeout of Hardware Cryptography Module
Anish Singhani
Carnegie Mellon University, United States

180 Attendees!! Record attendance among all workshops at VLSI Symposium

Open Source PDKs and EDAs, Community Experiences toward Democratization of Chip Design

Organizer : Makoto Ikeda (The University of Tokyo)å
Organizer : Mehdi Saligane (University of Michigan)

Since its launch in 2020, the Open MPW shuttle program has received over 500
to designers' experiences, including measured results, foundry perspectives, an

About Makoto Ikeda
Makoto Ikeda received his BE, ME, and Ph.D. degrees all in EE department of
d.lab, the University of Tokyo. This workshop is co-organized with Dr. Mehdi S

| 1. Design experience: "The Journey of Two Novice LSI Enthusiasts: T
Communications and Yuki Azuma, University of Tsukuba

| 2. From Zero to 1000 Open Source Custom Designs in Two Years, Mo

| 3. The SKY130 Open Source PDK: Building an Open Source Innovation

| 4. Open Source Chip Design on GF180MCU – A foundry perspective, Karthik Chandrasekaran, Global

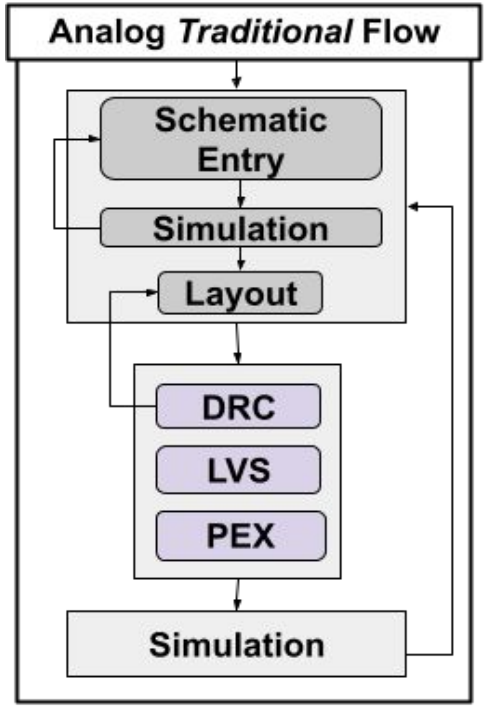
The End!

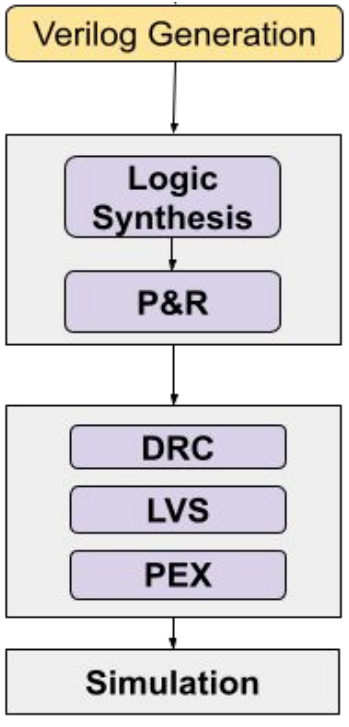
Traditional vs Automated Analog Design

Analog vs. Digital design flow

Automated

Manual/Custom

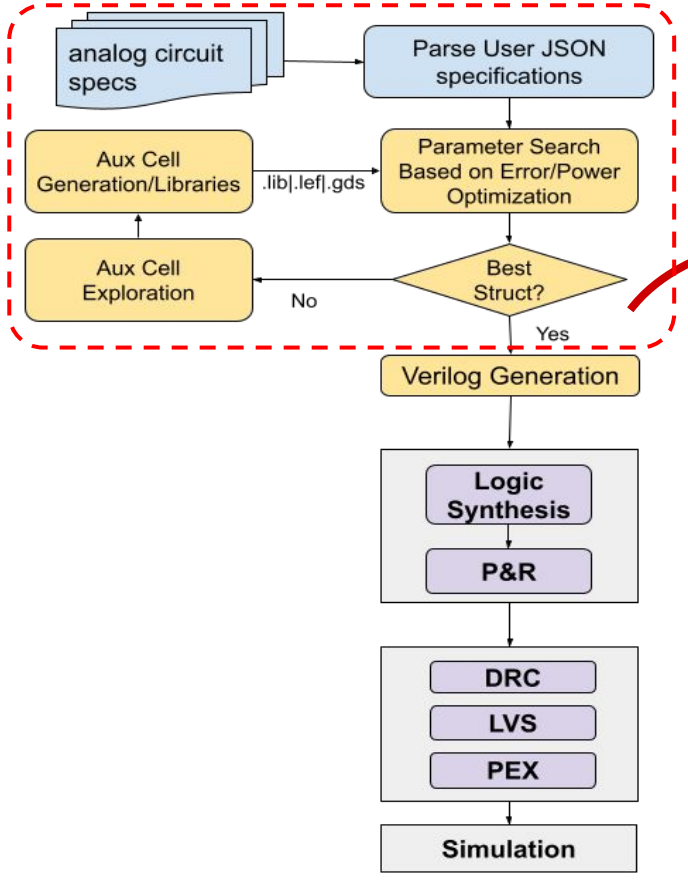




- **Analog** design flow
  *Significant number of **manual** and custom steps.*
- **Digital** design (*grid-based*) flow
  *Almost **entirely automated**.*

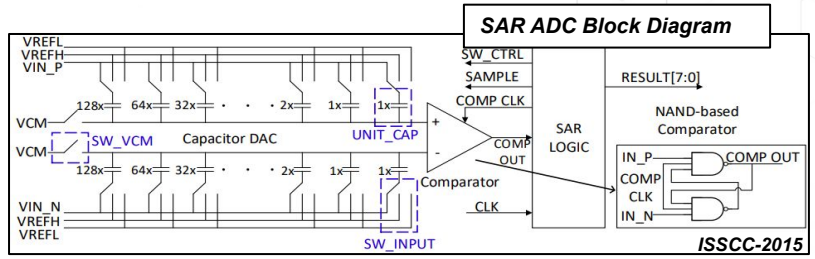
Generated Analog *into* Digital design flow

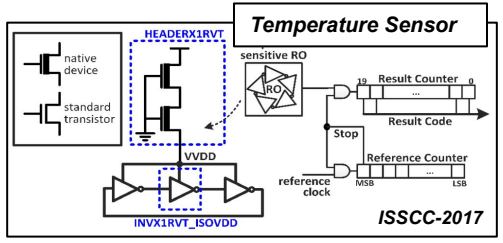
FASoC Generator

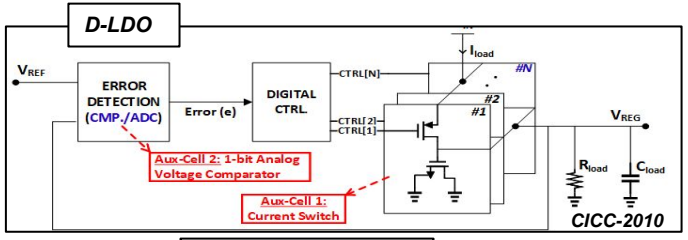


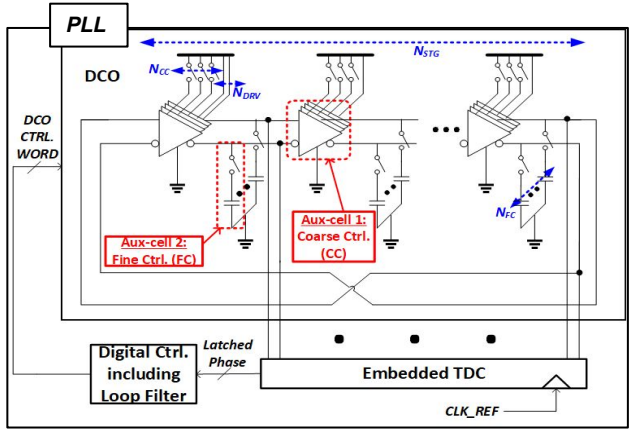
Automated

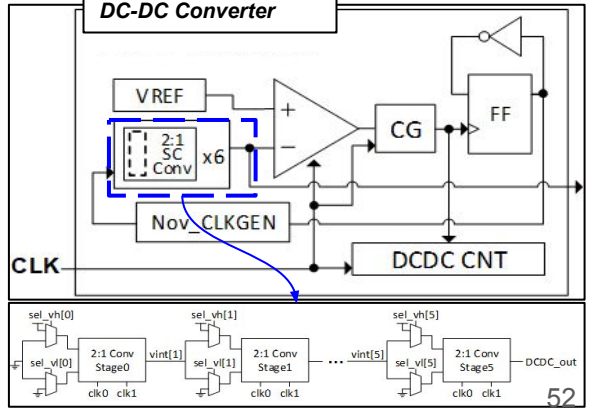
Manual/Custom





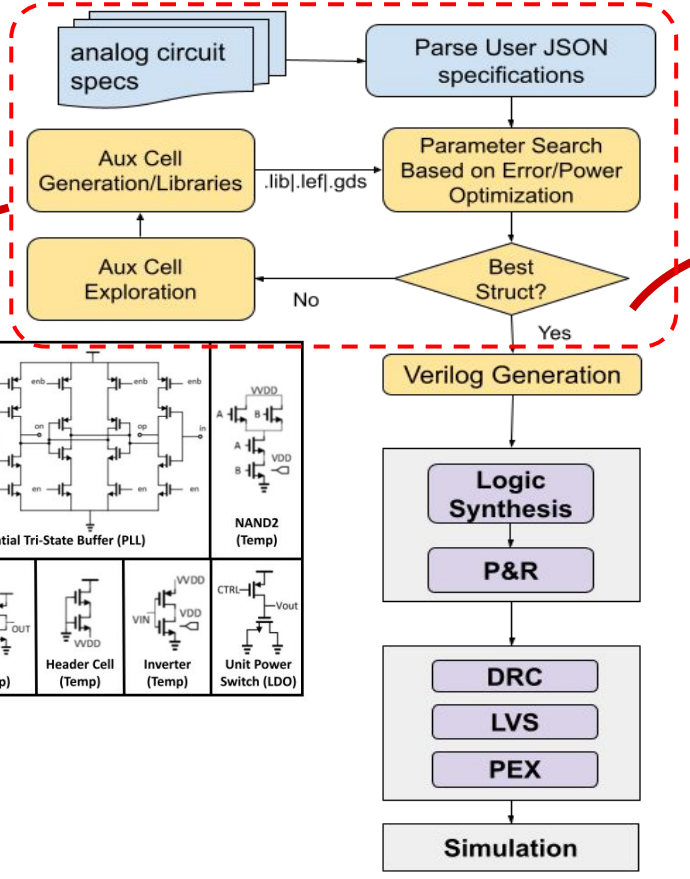


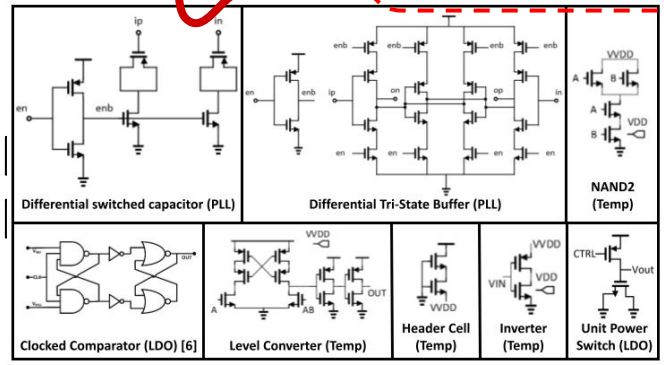


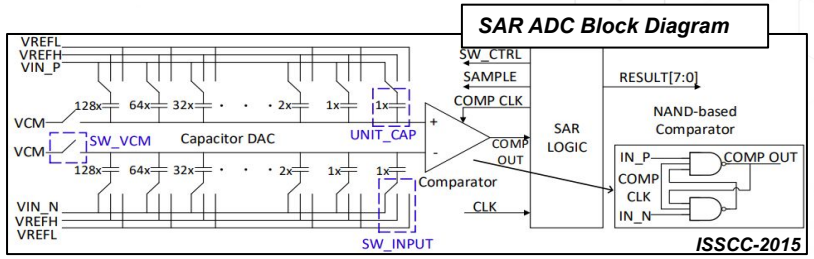


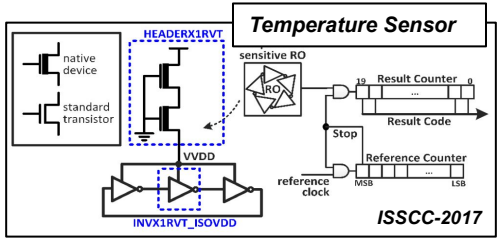
Generated Analog *into* Digital design flow

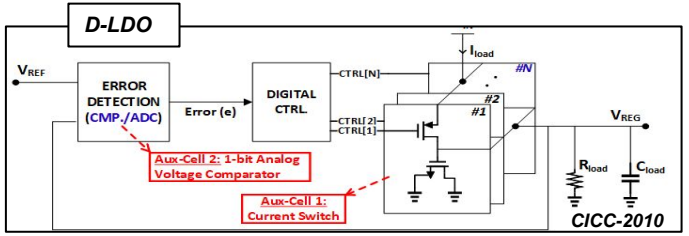
FASoC Generator

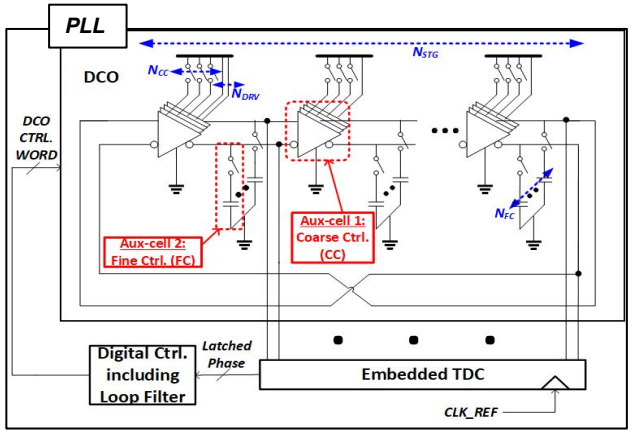


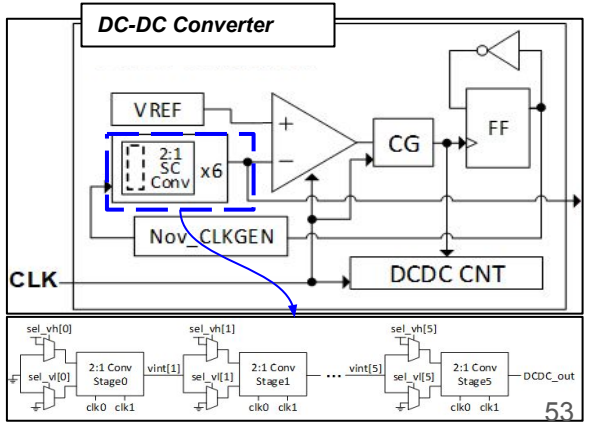






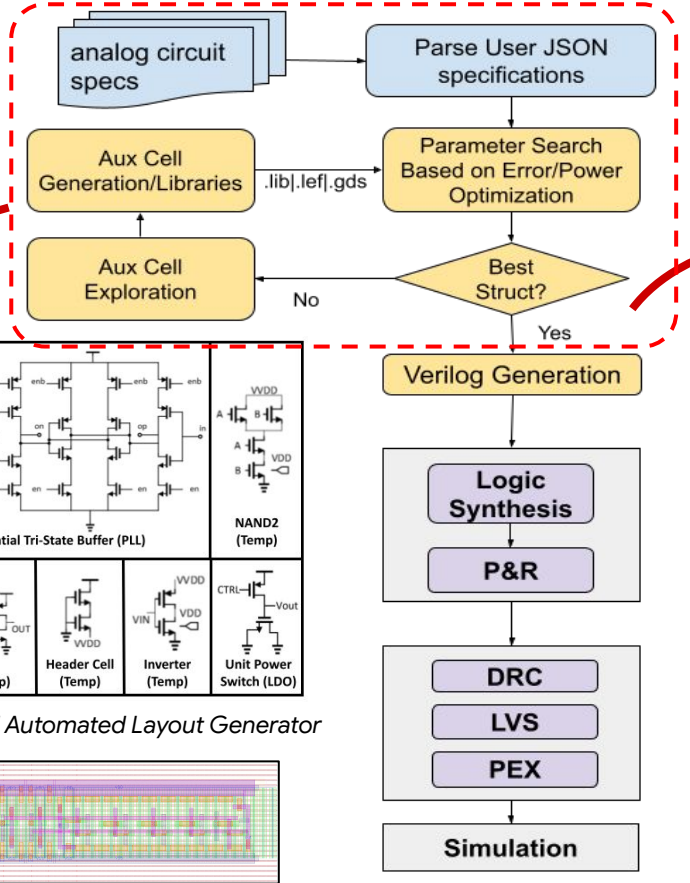


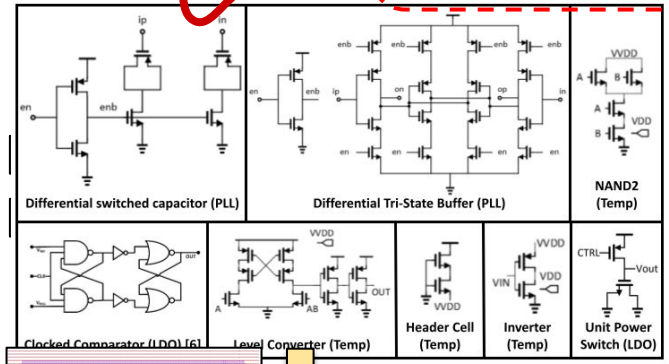




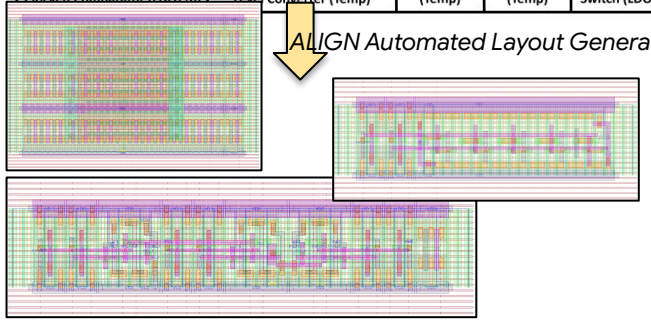
Generated Analog *into* Digital design flow

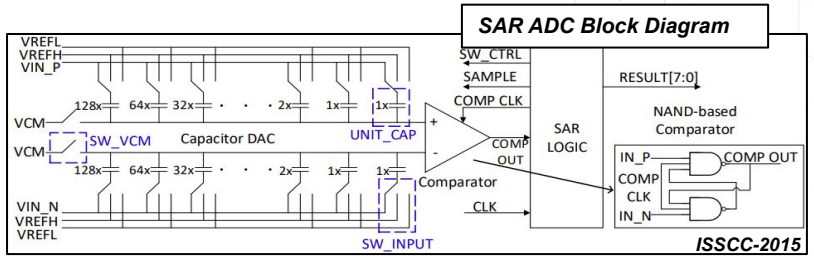
FASoC Generator

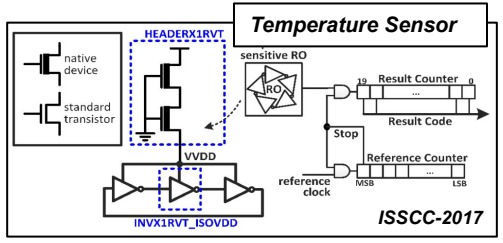


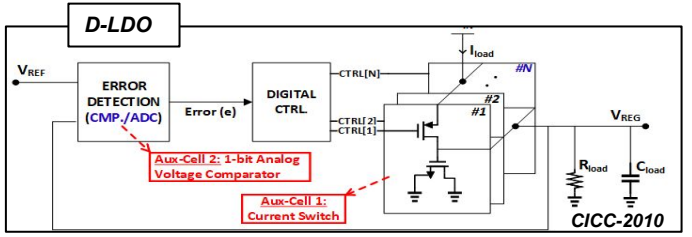


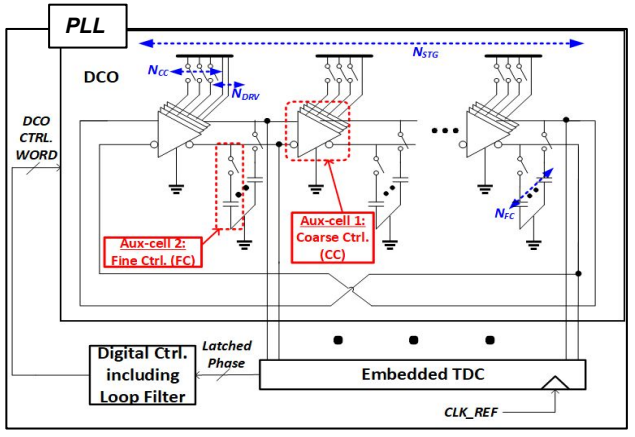
ALIGN Automated Layout Generator

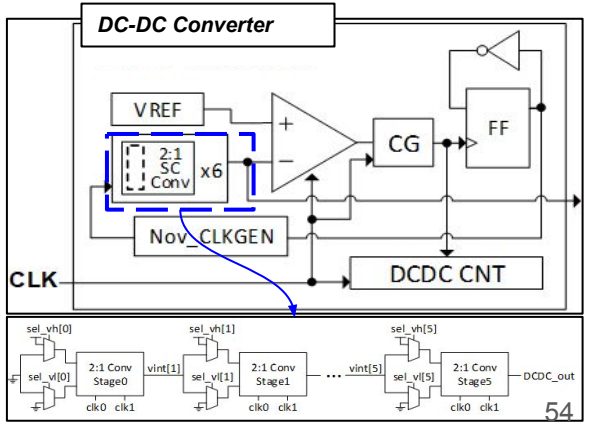












Initially only proprietary design flow