LiveHD and Anubis

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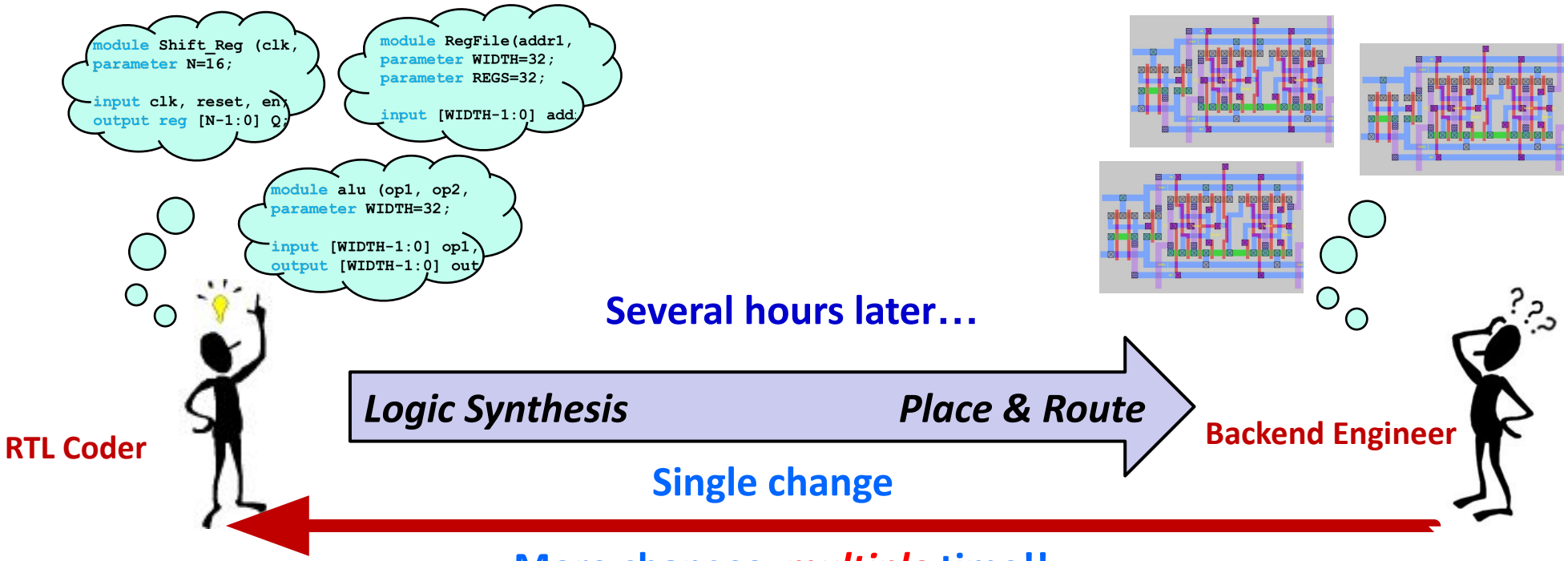
Outline

- ***Research Problem and Background***
- ***LiveHD***
- ***Anubis***
- ***Conclusions***

Current ASIC/FPGA Flow

- Re-compiling small design changes …… takes like forever
- v.s Software development

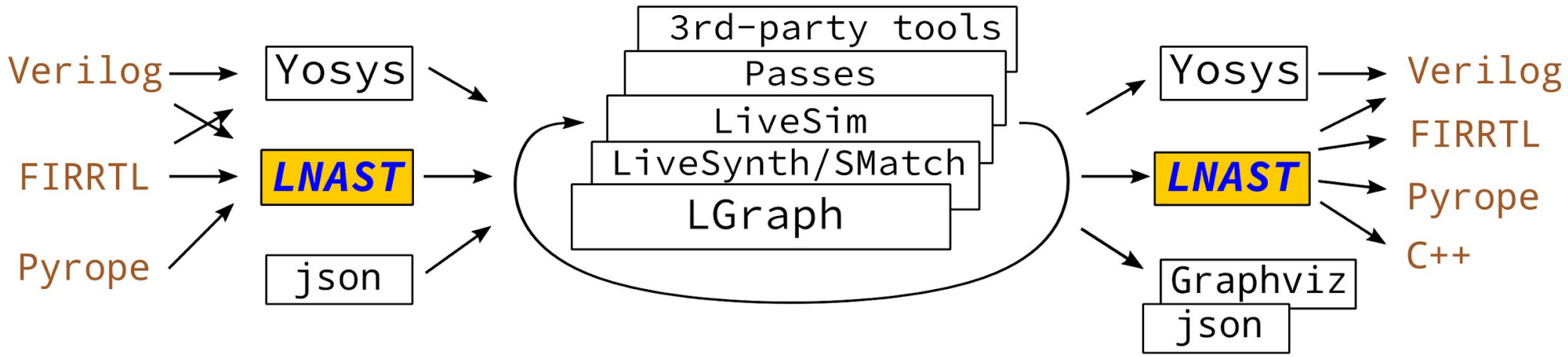


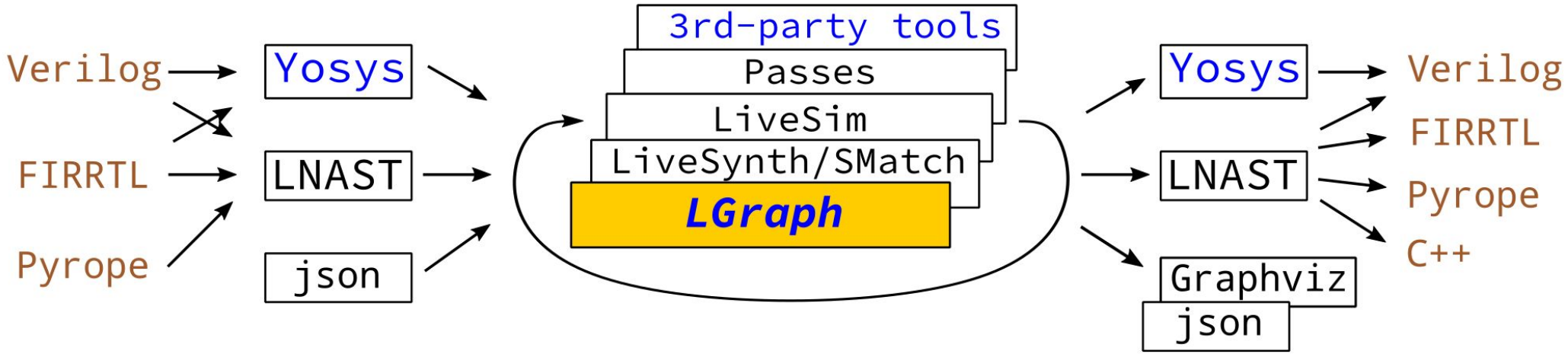
Live Hardware Development

- **LiveHD: incremental and scalable hardware design framework**
  - incremental: within "seconds", get feedback from small code changes
  - scalable: compilation, simulation, and synthesis for large design

- **Infrastructures: LLVM-like development ecosystem**
  - LGraph IR (WOSET'18, 19)
  - LNAST IR (WOSET'19)

LiveHD Two Level IRs: LNAST/LGraph





ANUBIS

- The first benchmark suite intended for evaluating incremental synthesis techniques and flows.
- Goal: Equivalent to the popular SPECint benchmark. typically used to report performance numbers in CPUs
- R.T. Possignolo, N. Kabylkas, J. Renau, "Anubis: A new benchmark for incremental synthesis" International Workshop on Logic and Synthesis '17

Conclusions

- Developing Fast and scalable code base for LiveHD
- Developing our Pyrope HDL based on LiveHD
- Multi-language interfacing
- Moving towards unified compiler for entire hardware design flow
- Anubis: To Benchmark the incremental flow

Questions?

https://github.com/masc-ucsc/livehd

https://github.com/masc-ucsc/anubis