Open-Source EDA and Benchmarking Summit

DAC-2022 Birds-of-a-Feather Meeting
Tuesday, July 12, 2022 7:00pm

Organizers: Andrew Kahng and Tom Spyrou

https://open-source-eda-birds-of-a-feather.github.io/

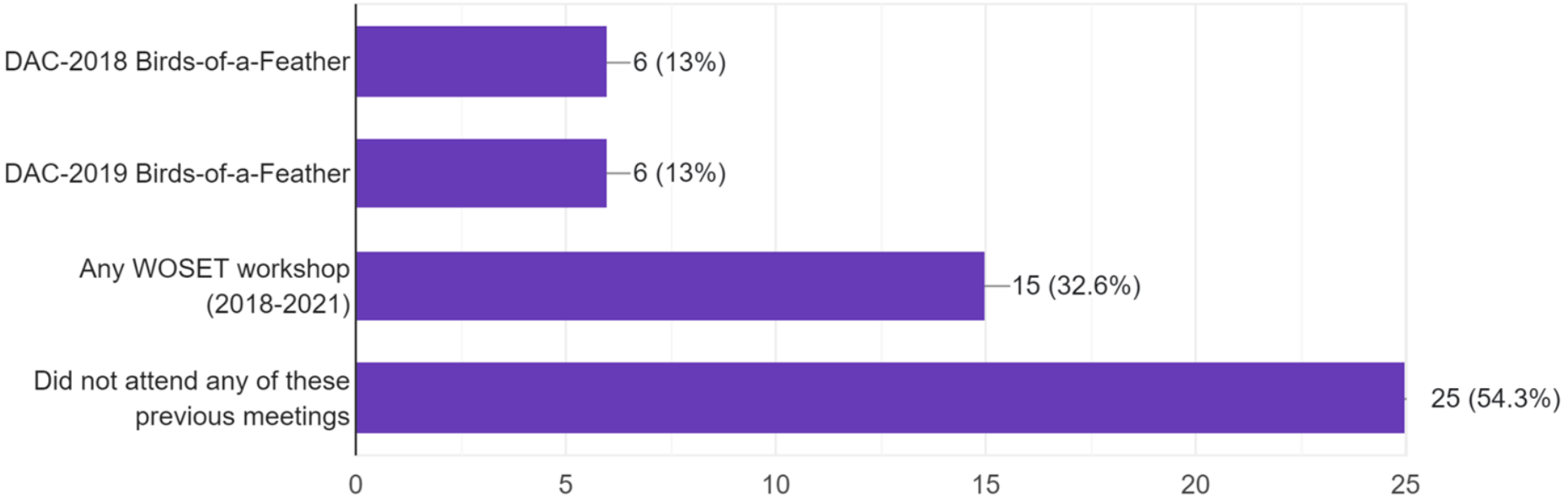
About This Meeting

- Third in a series of DAC Birds-of-a-Feather meetings: 2018, 2019 … **2022**
- **See: https://open-source-eda-birds-of-a-feather.github.io/**
- **Informal meeting point to share ideas and latest news**
- **Topics:**
  - **Ecosystem of open-source EDA tools**
  - **Use of relevant and principled benchmarking methodologies**
  - **Overarching goal: clarify and accelerate the leading edge of EDA research**
- **Today:**
  - **Current landscape and key updates**
  - **Goals for the community**
  - **Potential next steps / action items**

Planning Form - 48 responses, thank you !

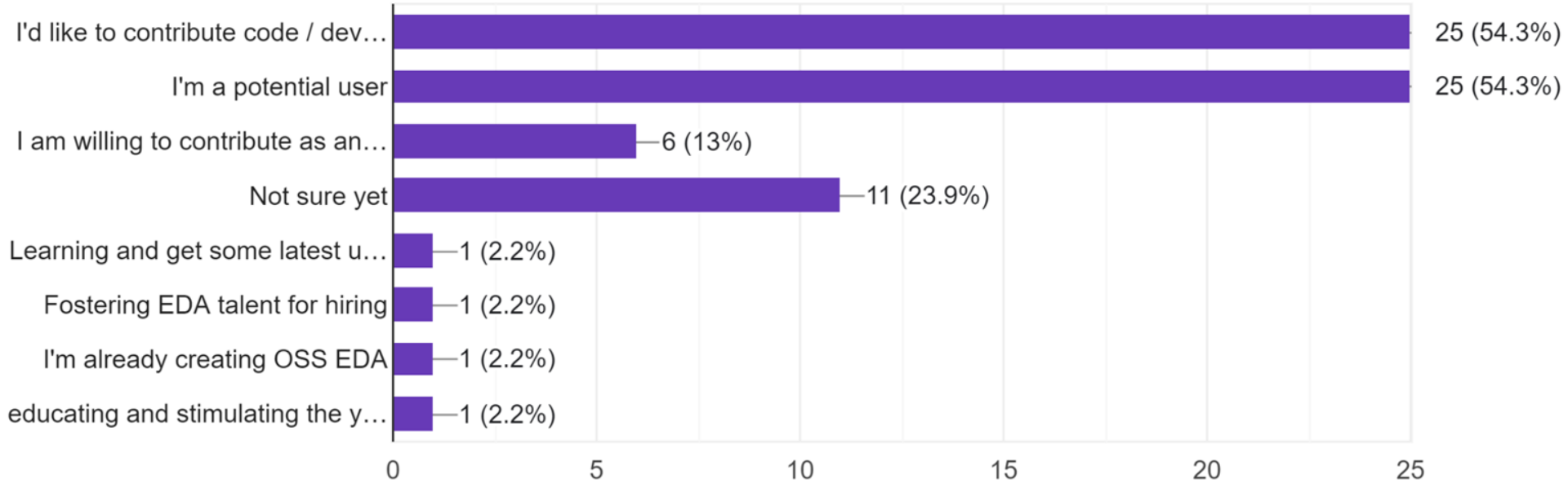
Which of these previous meetings did you attend, if any?

46 responses



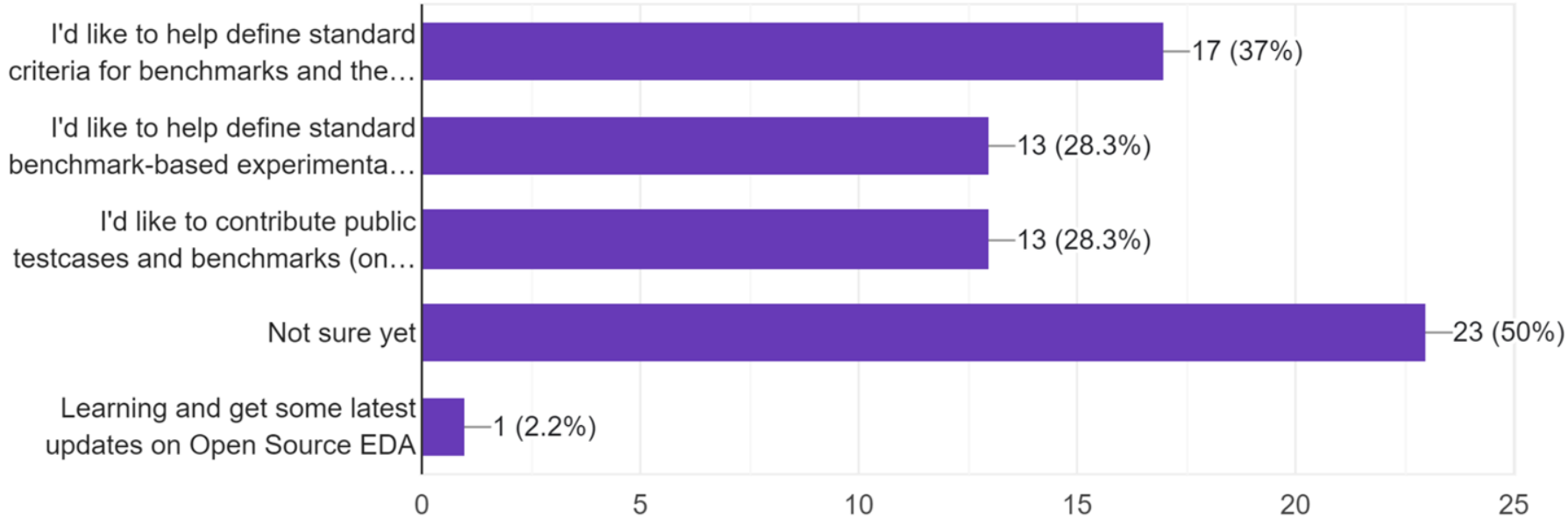
What is your interest in open-source EDA software?

46 responses



What is your interest in benchmarking of (academic) EDA?

46 responses



What would you most like to see discussed at the meeting?

Open-source EDA

- Current development of open-source EDA tools
- State of open source tools, and priorities/initiatives being planned.
- The path forward for open source community
- (1) Will open source EDA develop into an ecosystem that depends not just on volunteers at universities but where also commercial companies get established, providing e.g. support / tool certification for certain applications etc.? (2) Perspectives on open source IP libraries (e.g. RISC-V based) - will they become part of an open source design ecosystem?
- I am curious to learn more about the OpenROAD initiative and open-source API standards that allow "plug-and-play" in the PD flow along with data harvesting.
- What's the impact of OSS to chip design for the next 20 years.
- Real experiences of different open source usage models
- Educational activities and advocacy movements worldwide for Open-Source EDA.
- What prevents companies from not only adopting OSS EDA but also contributing to it?
- Opensource EDA tools impact on the CHIPS ACT

Data and Benchmarking

- Verification, standard benchmarks
- Analog design benchmarks
- Come up with a distributed way to "maintain" designs submitted to Open MPW at scale (much like GNU/Linux distributiion packagers manage to maintain an impressive amount of FLOSS software packages)
- (1) Elements and commitments of data and benchmarking infrastructure that enable the field to transparently move forward. (2) Key ("core") optimization problem statements that are the most important for the field to advance. (3) Open enablement of machine learning to advance optimization methodologies.

Machine Learning

- How can we accelerate adoption of ML in chip design processes?

Agenda Part 1: Open-Source EDA

- “OpenROAD: 3 Years in Perspective” – Tom Spyrou, UC San Diego and Precision Innovations
- “SiliconCompiler” – Andreas Olofsson, Zero ASIC
- “Parameters exploration using Jupyter notebook and Google Vizier – Johan Euphrosin, Google
- “Showcase and updates of the EPFL logic synthesis libraries (https://github.com/lsils/lstools-showcase)” – Siang-Yun (Sonia) Lee, EPFL
- “LiveHD and Anubis” – Sakshi Garg, UCSC
- “System-level tools (e.g., Instruction Set Simulator) recently open-sourced” – Ulf Schlichtmann, TU Munich
- “DFiant cloud solution that offers access to OSS EDA flows” – Oron Port, DFiant
- Late-Breaking News and Discussion (what next, what is needed, who can contribute …)

Open-Source EDA - Discussion

- Warren Savage: How do we get the foundries to support **OSS** ?
  - **Please ask your foundry of choice to enable “the OpenROAD kit”, for example**
  - [Signoff / verification were not in the original IDEA scope for digital implementation]
- Kerim Kalafala: Path forward to an ecosystem?
  - **From industrial perspective, with own tooling/process/methodology – how dis-integratable is something like OpenROAD? [Match to OpenSTA API, integrate to ODB, listen for callbacks …] (How badly do you want this?)**
  - See: RosettaStone OpenROAD
- Kevin Cameron: Standards (APIs, data) are ~locked in by big EDA players. **Need a new standards body for OSS EDA to replace pay-to-play Accelera, IEEE SA (cf. OCP for SDHW example) open standards? [SV focus of question]**
  - Kerim leads the SPEED API work at SI2 (API for “derived data”). (OpenAccess is for design data.)
  - [Standard question: “Is OpenAccess is really open?”
- Antonino Tumeo: Will the CHIPS Act and the DoC/NIST National Semiconductor Technology Center (NSTC) help with the foundries/ecosystem questions?
  - DoD uE Commons as well as “workforce development”
  - Hardware system innovation does require OS EDA. (Cf. Peter Gadfort et al.)
  - But, training chip designers with the U.S. version of EuroPractice / CMC does NOT require OS EDA
- **Ethan Mahintorabi ethanmoon@google.com : Trying to robustify OpenROAD at Google. Throwing down the gauntlet tonight: Lots of big companies on the signup list – who’s running designs through OpenROAD, filing issues, making PRs, … ?**
- Real experiences and impact on chip design?
- Educational initiatives and advocacy?

Agenda Part II: Data and Benchmarking

- “FPGA macro placement benchmark suite” – Ismail Bustany, AMD
- “New repository of benchmarks and best results targeting superconducting electronics (https://github.com/lsils/SCE-benchmarks)” – Siang-Yun (Sonia) Lee, EPFL
- “Efforts toward open data and benchmarking in the TILOS AI Institute: MacroPlacement and SpecPart” – Andrew Kahng, UCSD
- “Circuit Training (https://github.com/google-research/circuit_training), the open-source library for floorplanning using RL that my team and Google has open sourced recently as described in the ‘A graph placement methodology for fast chip design’ paper” – Sergio Guadarrama, Google

- Late-Breaking News and Discussion (what next, what is needed, who can contribute …)

Data and Benchmarking – Discussion 1/2

- Johan (Proppy): Results in academia are generally incomparable !
  - (Um, yes ….. That's a cultural aspect of VLSI CAD research)
- Kerim: Would be great if we had benchmarks that were representative of commercial leading-edge problems (complexity, corner cases, objectives, etc. – but, protective of commercial entities' IP)
  - How? → Anonymization, Obfuscation, Artificial [um, but this takes effort …]
  - Ethan: Is an old (complete) design still all that (strategically) valuable today?
- What is a benchmark?
  - E.g., "golden" somehow
- Should benchmarks be "retired"?
  - E.g., ISCAS85, MCNC
- **Should EDA research be reproducible? (yes)**
  - Igor: (i) By the authors? (yes) (ii) By others? (yes, if they have the same code and data and resources) (iii) Independent reproducibility from the code
- **How can EDA research "at the leading edge" be reproducible?**
  - Is there any point to do work on "advanced nodes"?
  - An "**svtests**" for other domains? ← Google came up with this, AntMicro did a lot of work (recall CSS testing)
- **What incentives exist for this "culture change"? (reproduction …)**
  - **ML community asks for collaterals that increase reviewer confidence in the results**
  - **(ICCAD-2022 did this) ("submit notebooks, not pdfs")**
- Questions re CT talk
  - Will you release any pre-trained model (e.g., suitable for Ariane-133)? (Will check)
  - What is the datapath structure / content like of the (TPU) testcases?
  - How were the better / same / worse comparisons adjudged? (By human experts)

Data and Benchmarking – Discussion 2/2

- Verification benchmarking
- Analog design benchmarking
- Principles, and how to enable the field to transparently move forward?
  - Data: enablements and designs that are “scalable and sharable”
- Core optimization problems that need progress
  - Forcing optimization out of comfort zones: → DL, cloud, … ; flow-relevant benchmarking, …
- Ethical, fair benchmarking
  - Transparency, openness
  - Figures of merit
  - Measurement processes
- Followups to survey: form working groups?
  - Define benchmarking methodologies
  - Provide benchmarks and data

Agenda Part III: New Research Foundations

- “Push for an Open Hardware Technology Commons in Coordination with the NIST National Semiconductor Technology Center” – Antonino Tumeo, Pacific Northwest National Laboratory
- “How persons developing flows and other work products can share those with colleagues” – David Junkin, Cadence

- Late-Breaking News and Discussion (what next, what is needed, who can contribute …)

Research Foundations - Late-Breaking News and Discussion

- Hardware commons?

- Sharable Sharing of scripts and reproducible research ?!?
  - **Will we require research results to be reproducible?**

- Working groups and volunteers?
  - Core EDA optimization problems (to benchmark and roadmap)
  - Key gaps in open-source EDA (to fill in)